

Model Name : B5V1L
File Name : LA-D921P

Compal Confidential

Braswell M/B Schematics Document

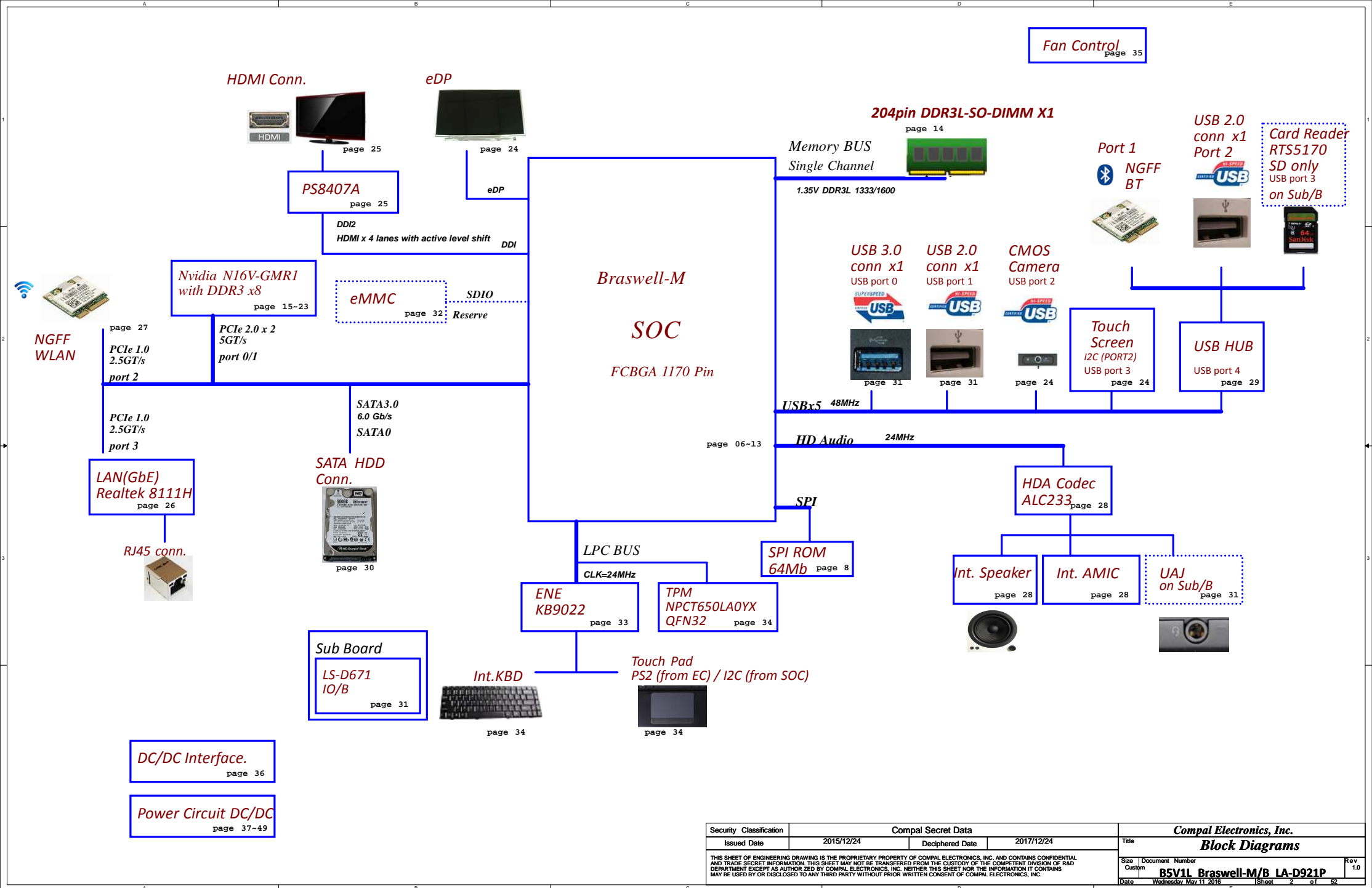
Intel Braswell-M DIS

B5V1L
LA-D921P REV:1.0
2016-05-04

PCB@
ZZZ PCB B5V1L LA-D921P LS-D671P

Part Number	Description
DAZ1QA00100	PCB B5V1L LA-D921P LS-D671P

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Power Plane	Description	S0	S3	S4/S5
+19V VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
+19VB	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	OFF
+1.15VALW	+1.15v Always power rail	ON	ON	OFF
+1.24VALW	+1.24v Always power rail	ON	ON	OFF
+1.8VALW	+1.8v Always power rail	ON	ON	OFF
+3VALW	+3.3v Always power rail	ON	ON	OFF
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+3V PTP	+3.3V power rail for PTP	ON	ON	OFF
+SOC VCC	Core voltage for SOC	ON	OFF	OFF
+SOC VGG	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA CORE	Core power for discrete GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
SOC_I2C0	Reserved (Touch Pad)			
SOC_I2C2 +3VALW	Reserved(Touch Screen)			
SOC_I2C5 +3VALW	Touch Pad SA577C-1202 (ELAN)	0x15		
	Touch Pad TM-P3218-001 (SYNAPTICS)	0x2C		
PCU_SMB +3VLAW	D MM1	0xA0		
EC_SMB_CK2 +3VS	N16V-GMR1 (VGA)	0x9E		
EC_SMB_CK1 +3VALW_EC	BQ24735R(Charger IC)	0x12		
	BATTERY PACK	0x16		

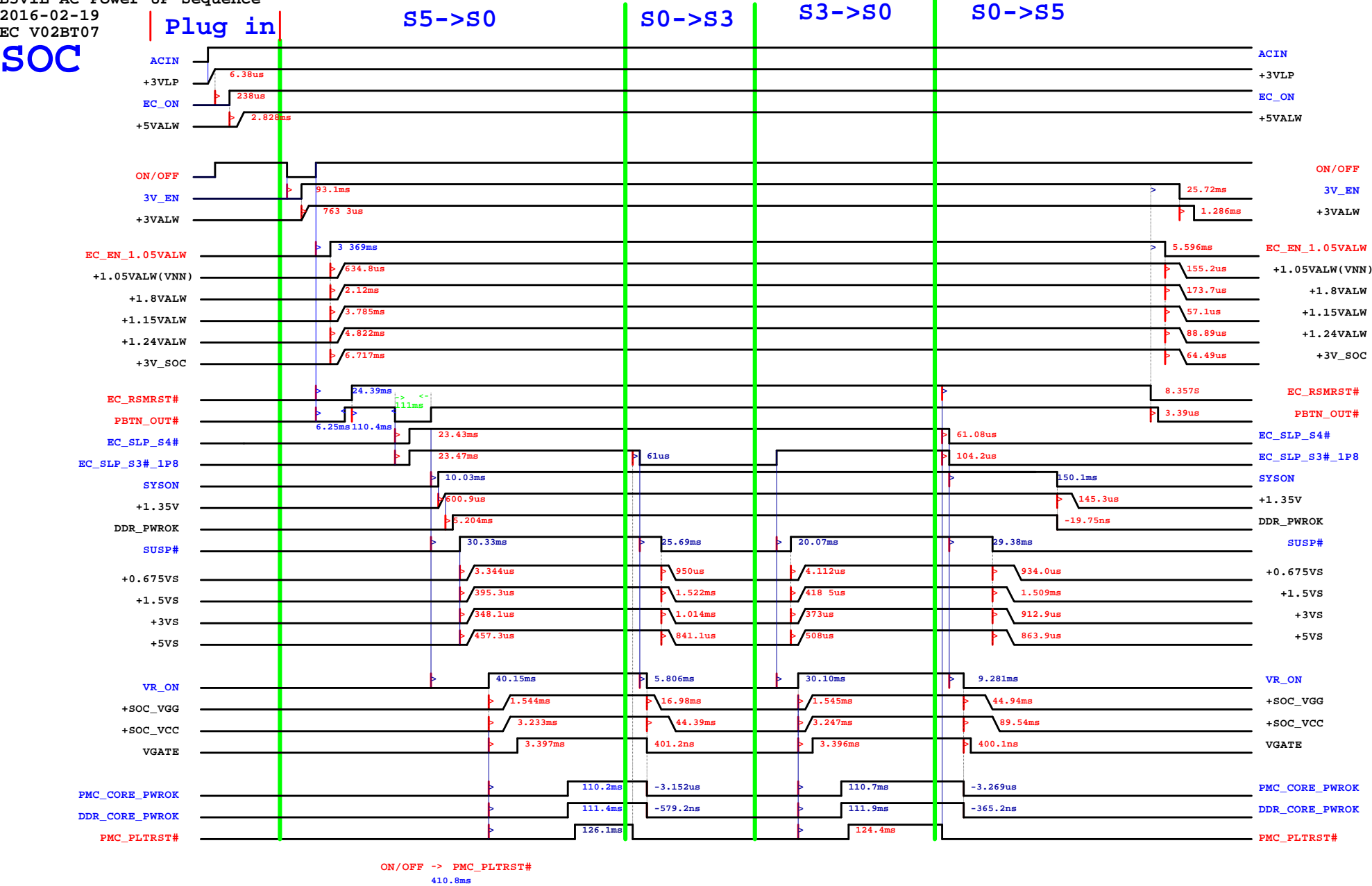
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xFE
19	NC	3.000V	3.300V		0xEF - 0xFF

[illegible]

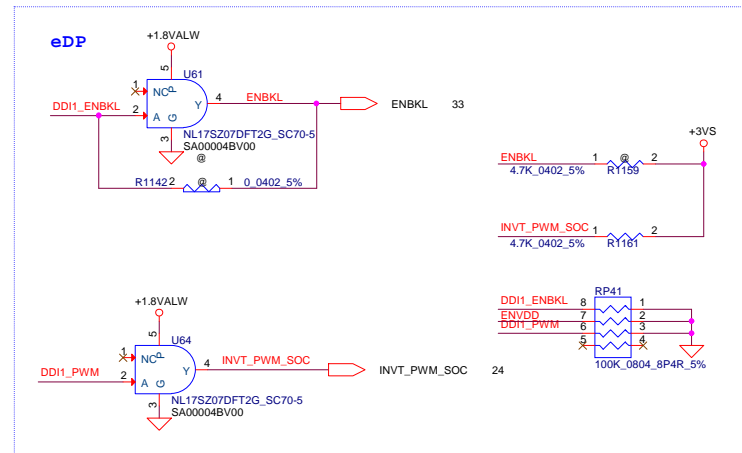
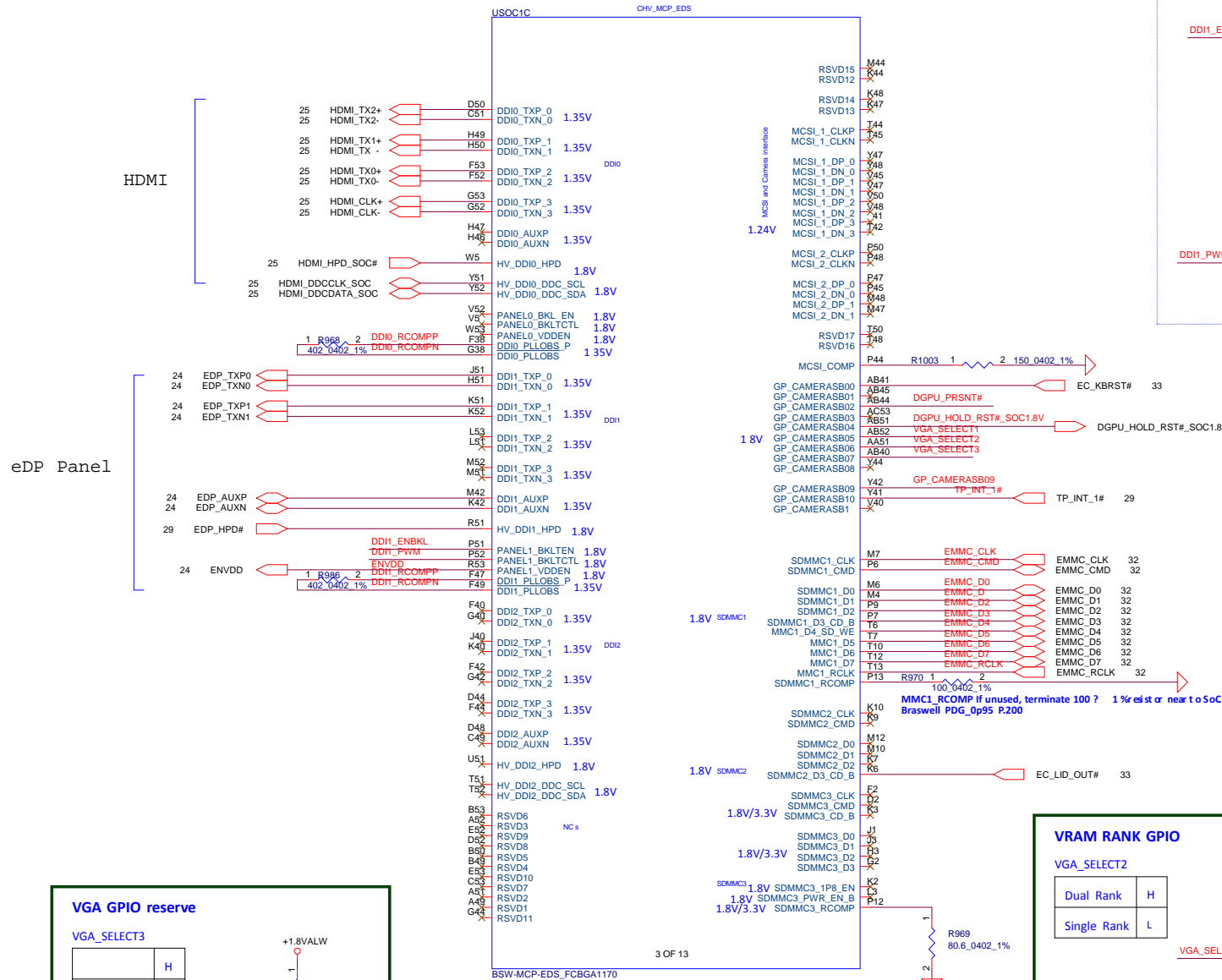
Item	BOM Structure	Item	BOM Structure	Item	BOM Structure
Unpop	@	USB HUB	HUB@	CPU 3060	QK0J@
Connector	CONN@	with BYOC	BYOC@	CPU 3160	QK0K@
EMC requirement	EMC@	without BYOC	NBYOC@	CPU 3710	QK0G@
EMC requirement depop	@EMC@	eMMC parts	EMMC@	CPU N3060	SR2KN@
HDMI active LS	ALS@	RTL8111GUS LAN	8111GUS@	CPU N3160	SR2KP@
Power Button	DBG@	RTL8111H LAN	8111H@	CPU N3710	SR2KL@
TPM	TPM@	Touch Screen	TSI@		
VGA	VGA@	N16V-GMR1	GMR1@		
Dual Rank	DR@	N16S-GTR	GTR@		

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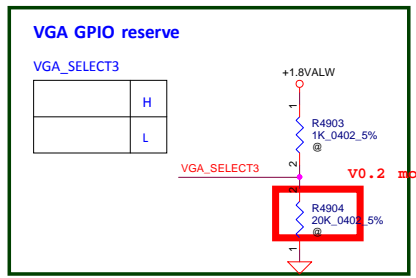
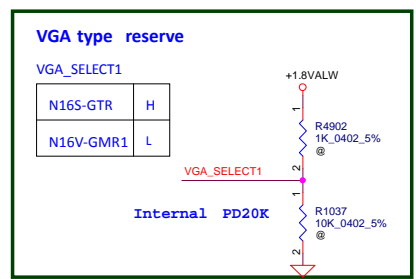
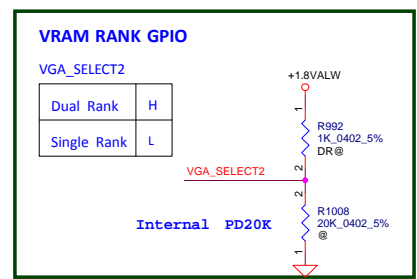
SOC

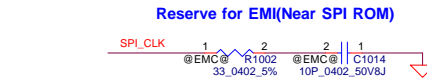
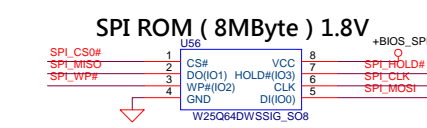
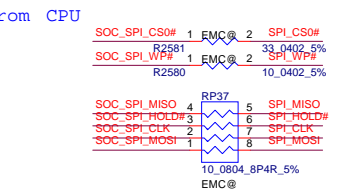
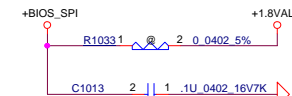
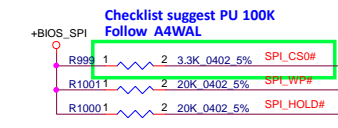
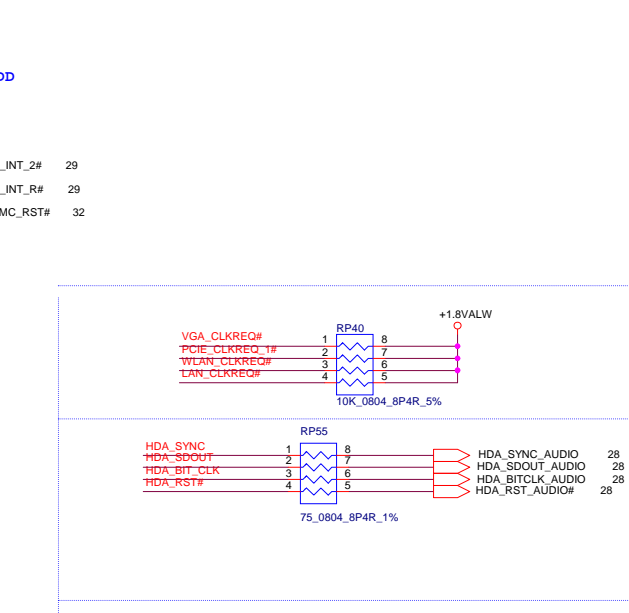
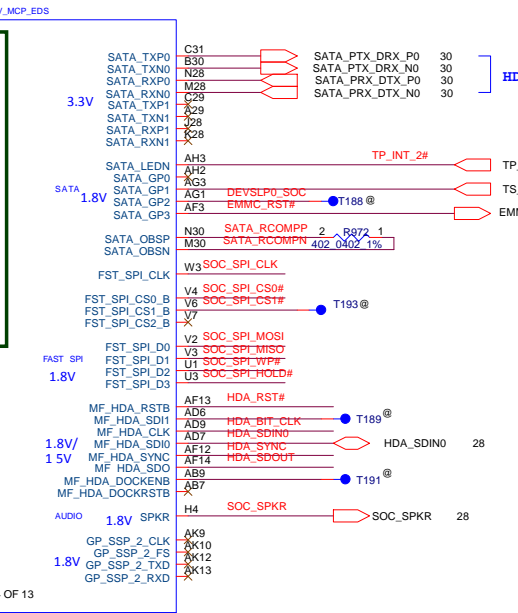
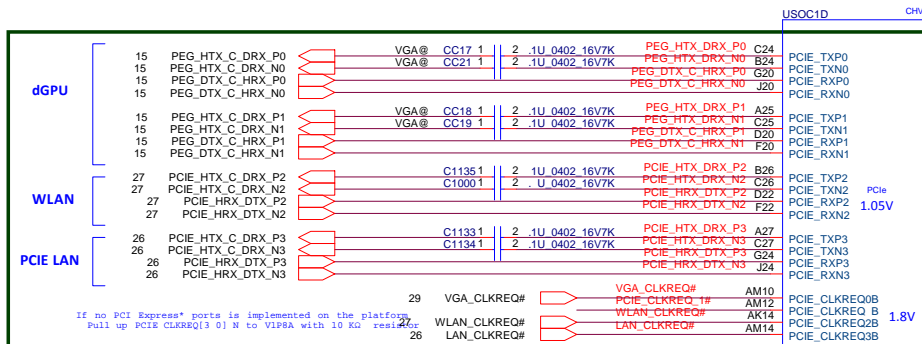


ON/OFF -> PMC_PLTRST#
410.8ms



DGPU_PRSN#	
UMA	H
DIS	L *

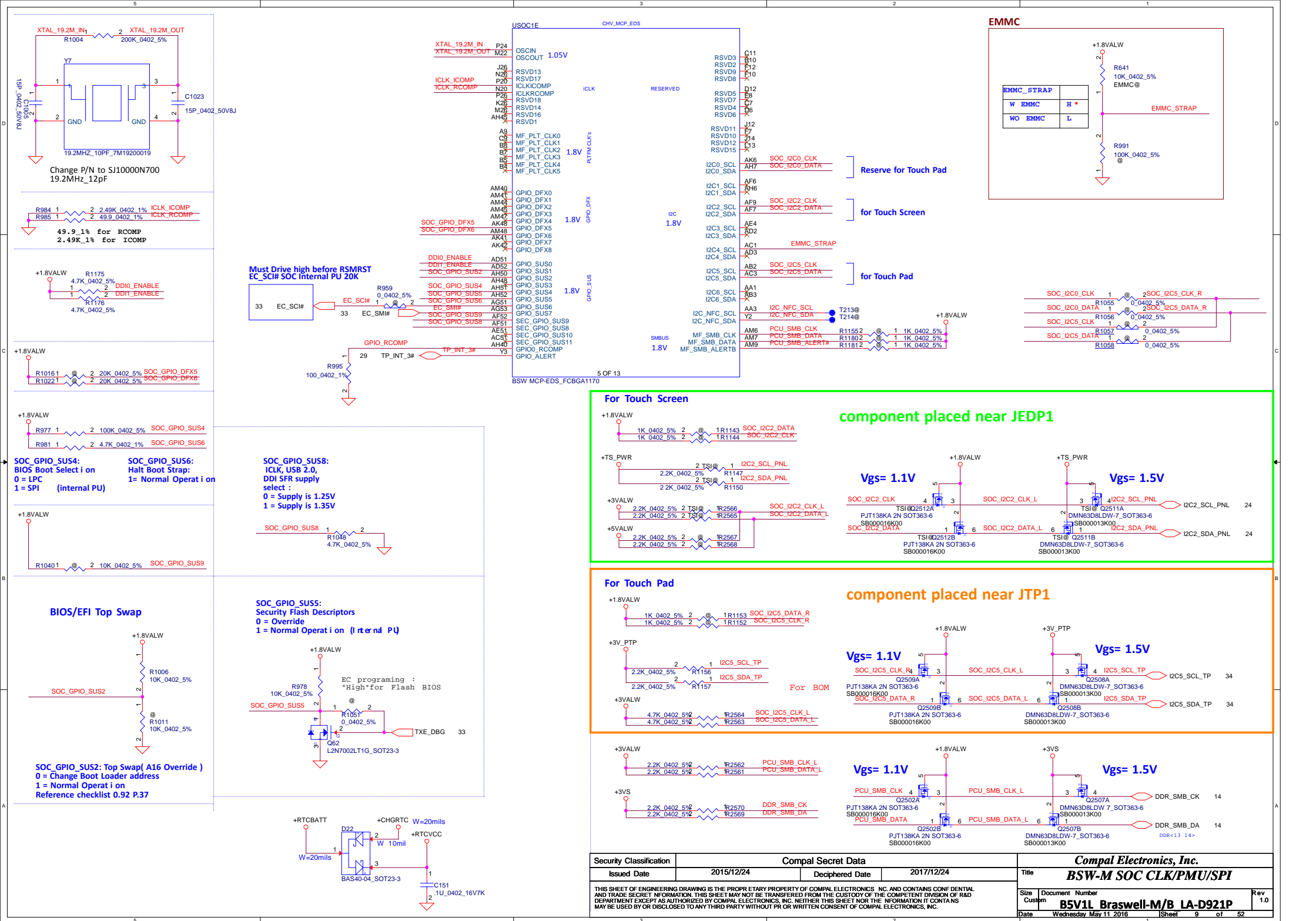


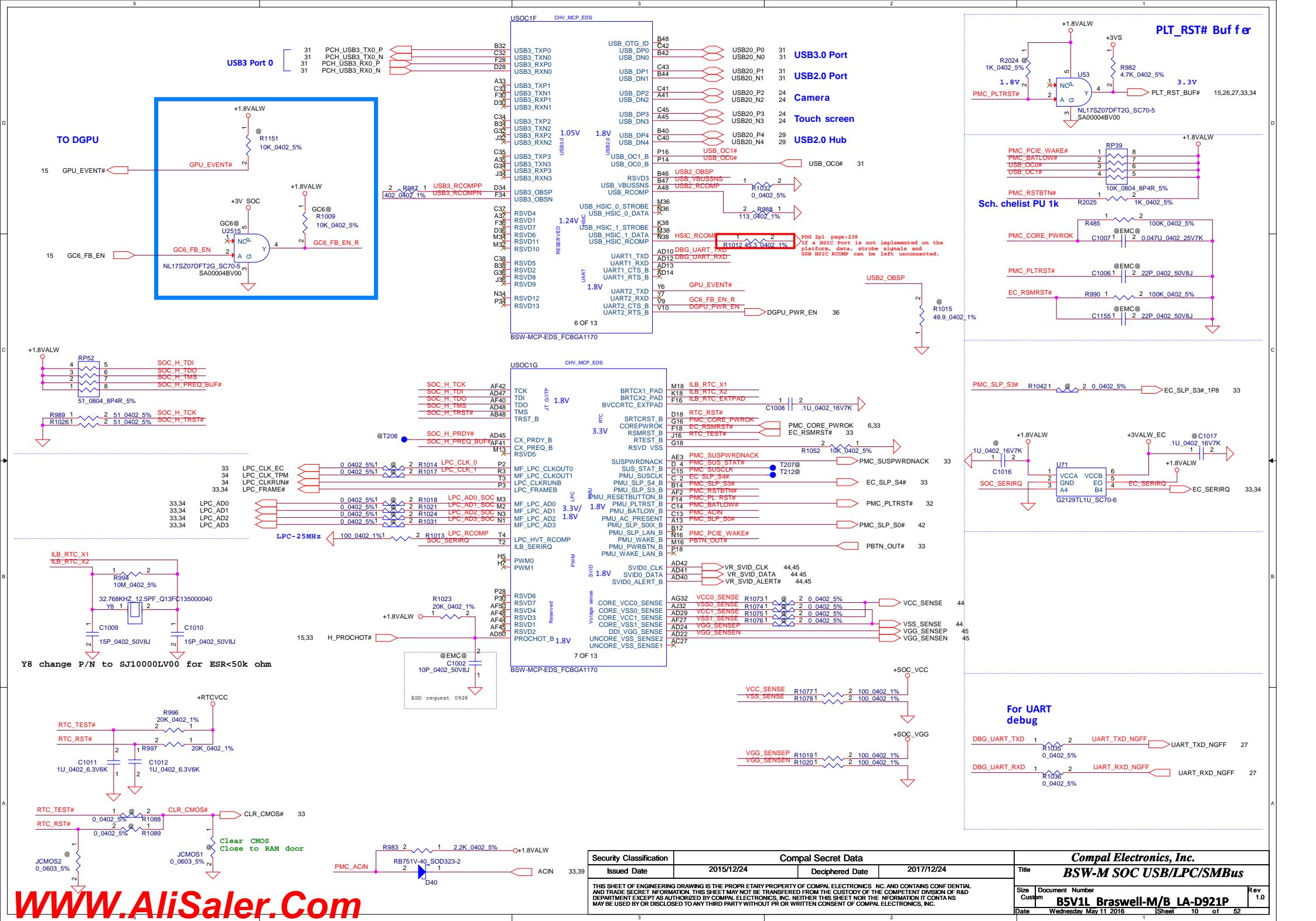


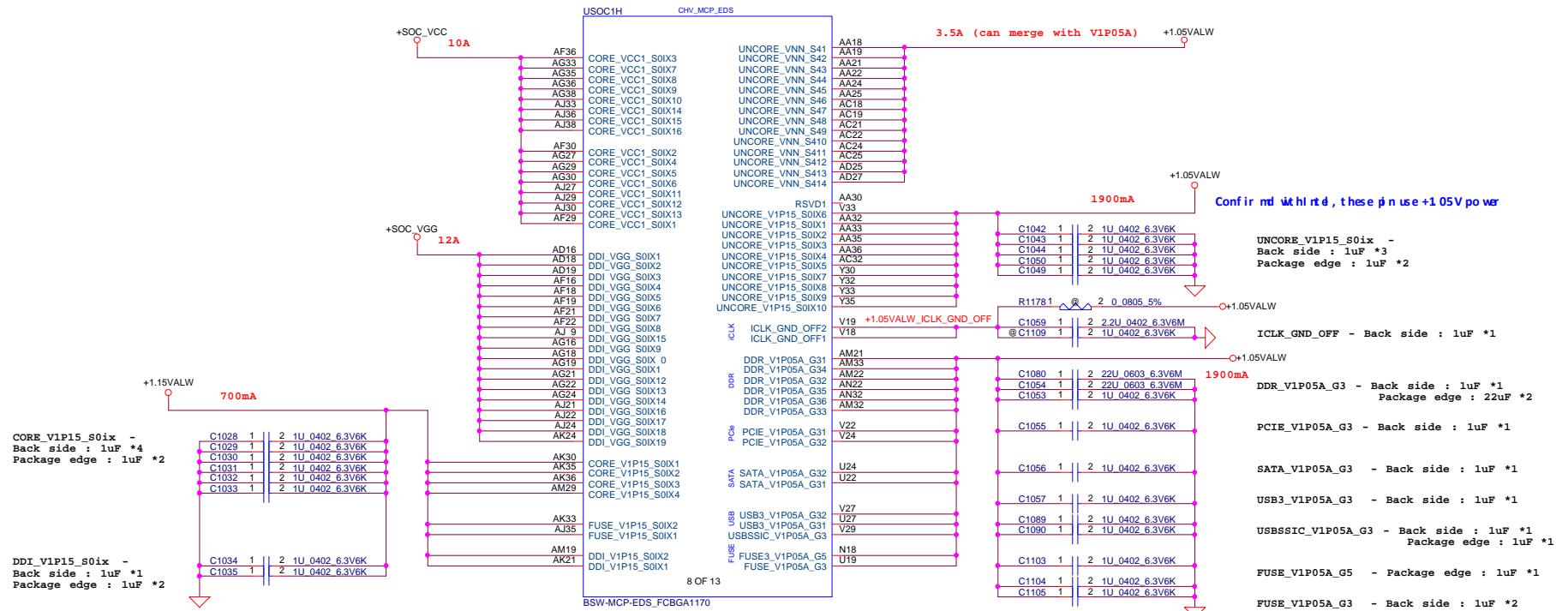
3.5.1 Intel BSW with USB20 Hub

Braswell	Acer
USB3 Port0	USB 3 (I/O)
USB3 Port1	USB 3 (I/O)
USB3 Port2	
USB3 Port3	
PCIe Port0	dGPU/M.2 PCIe LAN
PCIe Port1	WIFI
PCIe Port2	WIFI
PCIe Port3	LAN+CR
SATA0	HDD
SATA1	QDD
USB2 Port0	USB 3 (I/O)
USB2 Port1	USB 3 (I/O)
USB2 Port2	CCD
USB2 Port3	TS
USB2 Port4	USB HUB
USB HUB P1	BT (BT could connect to SOC if SOC has enough port)
USB HUB P2	USB 2 (I/O)
USB HUB P3	USB 2 (I/O)
USB HUB P4	USB CR
eMMC1	eMMC
SD2	
SD3	CR

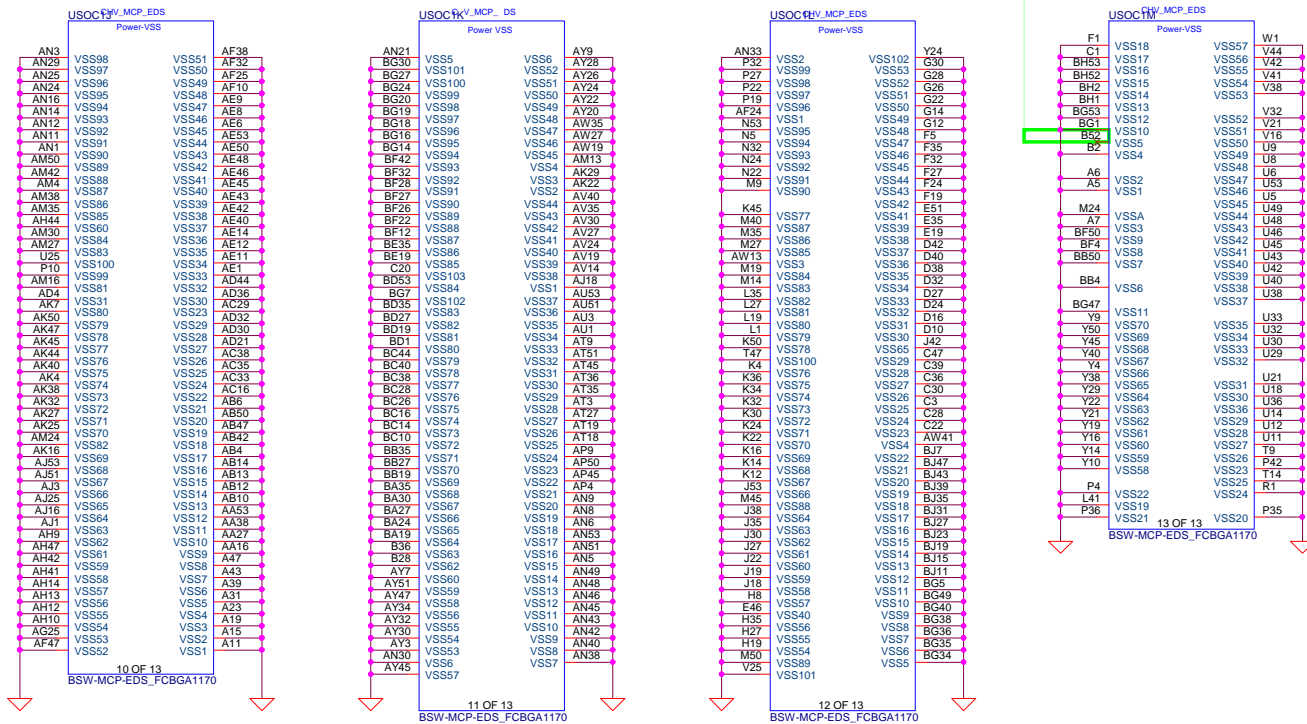
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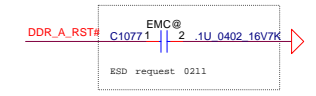
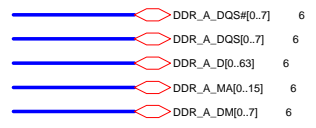
All VREF traces should have 10 mil trace width

Swap D4-->D5, D5-->D6, D6-->D4

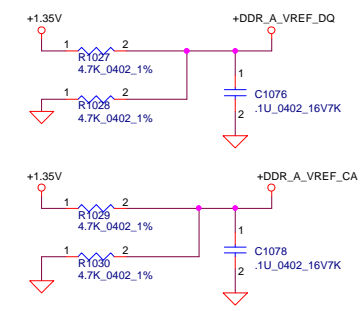
Channel A

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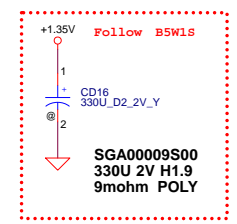
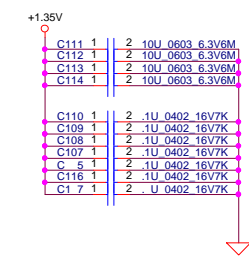
DIMM_1 Reverse



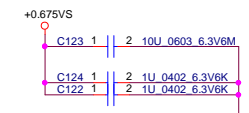
Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 u F placed close to VREF pins of each DDR3 SODIMM.



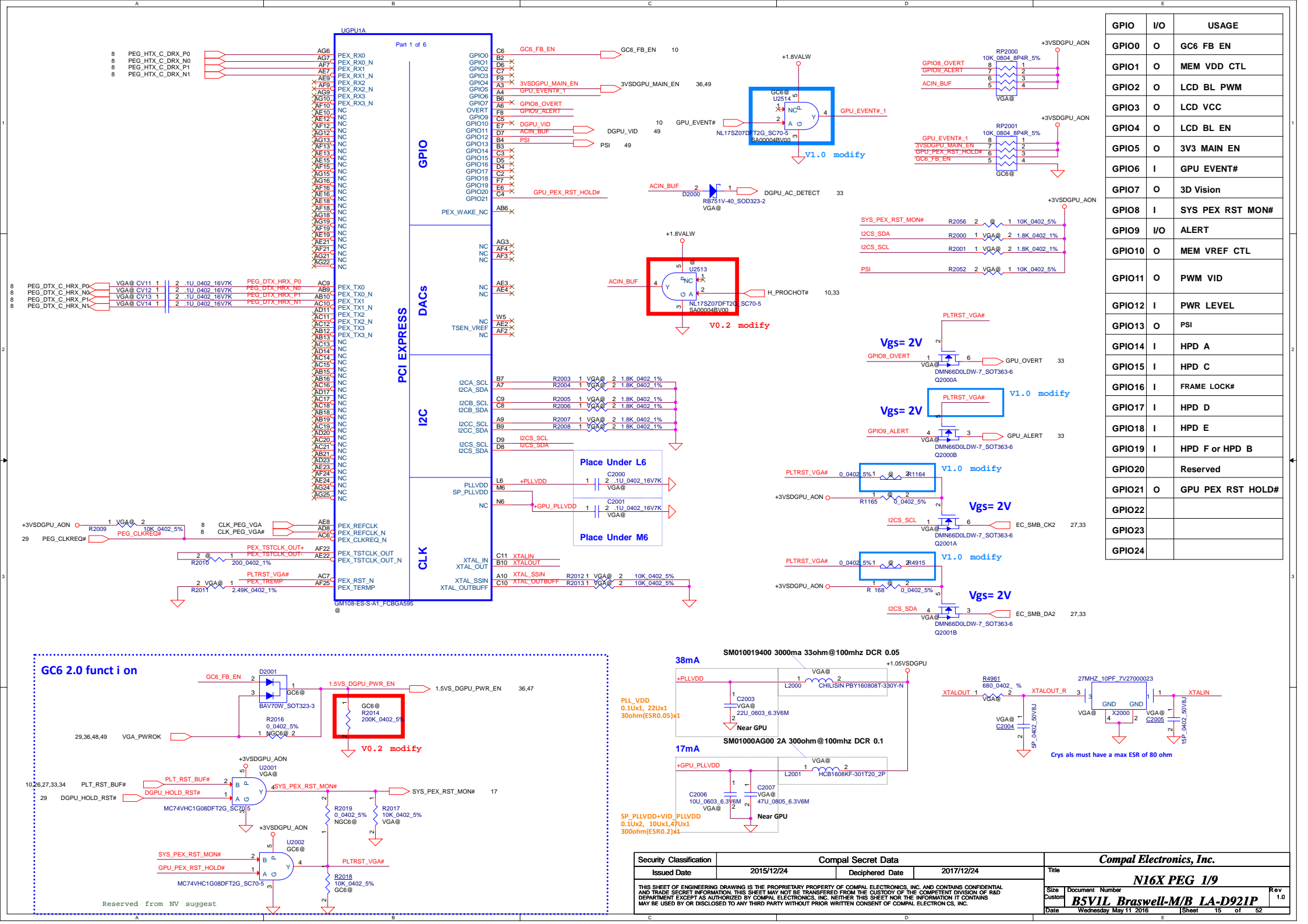
Layout Note
Place near JDIMM1



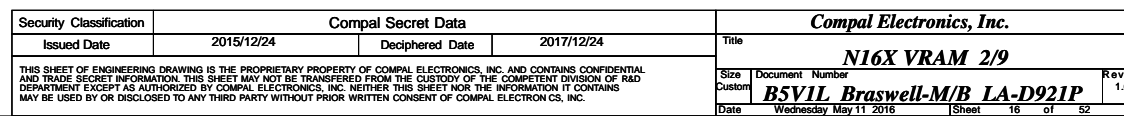
Layout Note
Place near JDIMM1.203,204

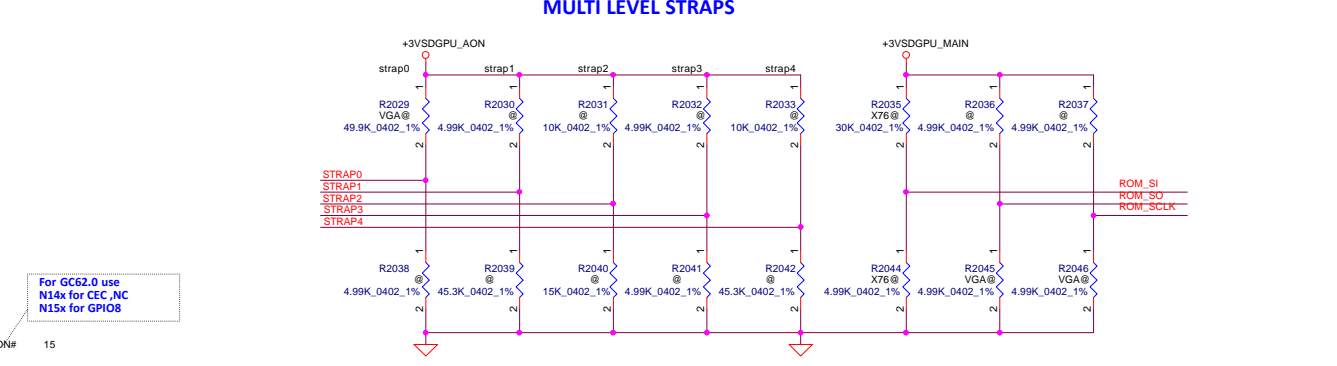
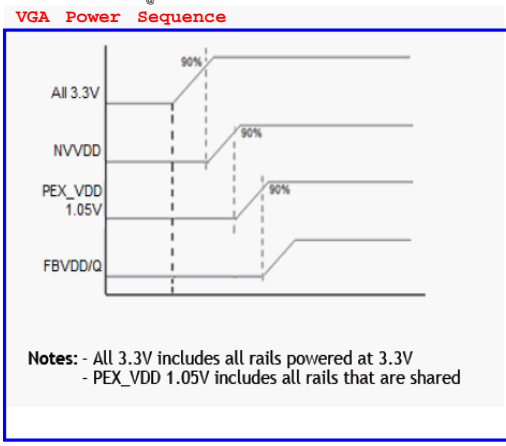
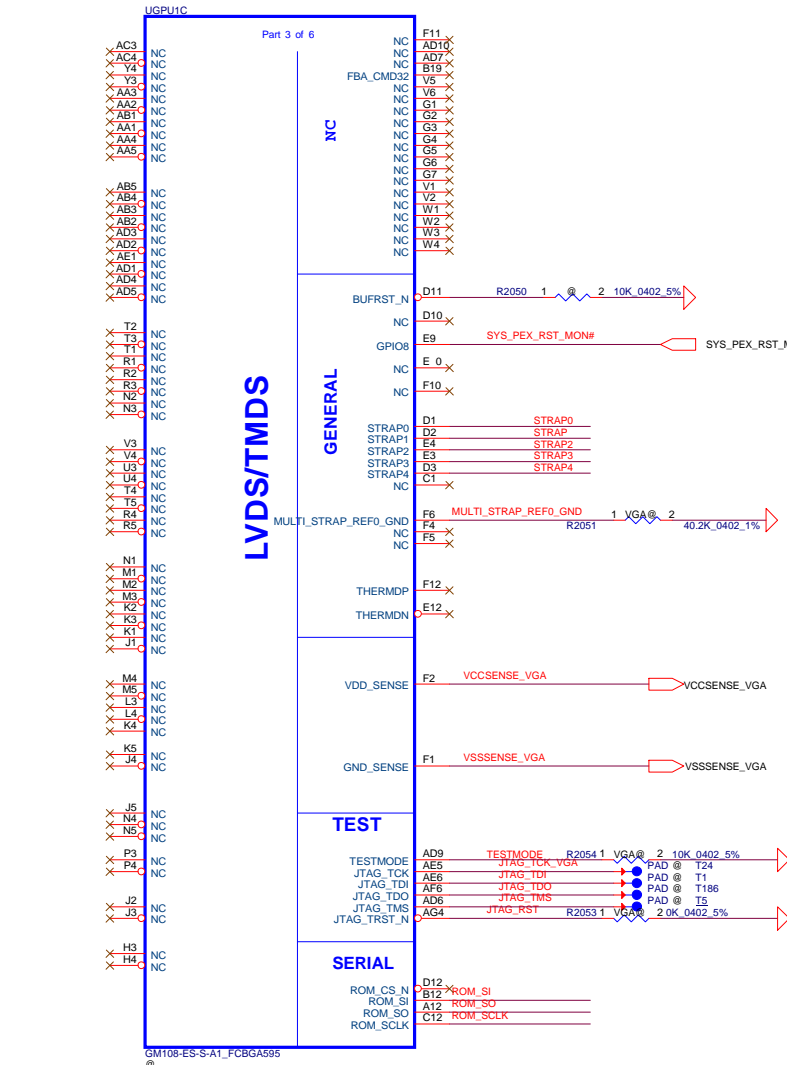


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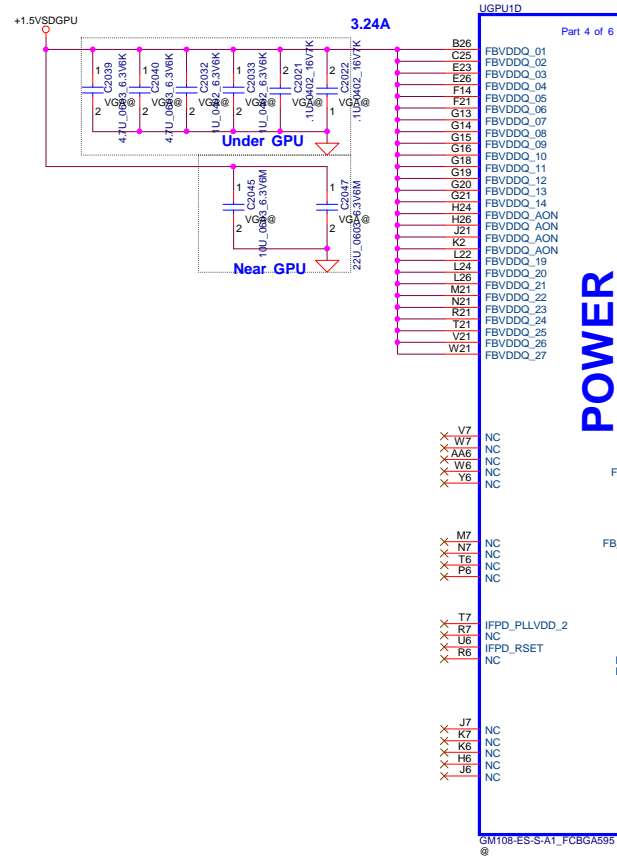
For N16V-GMR1 Multi strap table							Decive ID : 0x134F							
GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Conlig	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GMR1	+1.5 V	Dual	X76683B0003	1GH	256Mx16x8 4G	0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 49.9K	NC	NC	NC	NC	PU 24.9K	PD 4.99K	PD 4.99K
			0xD (SA00007PB0) Samsung K4W4G1646E-BC1A			PU 30.1K								
	X76683B0001	0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PD 15K											
	X76683B0002	0x4 (SA00007PB0) Samsung K4W4G1646E-BC1A	PD 30.1K											
	+1.5 V	Single		0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PD 24.9K									
				0x4 (SA00007PB0) Samsung K4W4G1646E-BC1A	PD 15K									

For N16S-GTR Multi strap table							Decive ID : 0x134D							
GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GTR	+1.5V	Dual	X76683B0005	1GHz	256Mx16x8 4G	0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 49.9K	NC	NC	NC	NC	PU 24.9K	PD 4.99K	PD 4.99K
			0xD (SA00007PB0) Samsung K4W4G1646E-BC1A			PU 30.1K								
						PD 15K								
	X76683B0004	1GHz	256Mx16x4 2G	0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PD 30.1K									
	0x4 (SA00007PB0) Samsung K4W4G1646E-BC1A			PD 24.9K										
				PD 15K										

NV 16x DG-07158-V05

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

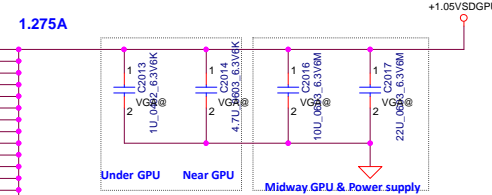
GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU



NV 16x DG-07158-V05

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply



NV 16x DG-07158-V05

GPU Package	Rail	Capacitor Type		Footprint	Population		Location
GB2B-64	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU

POWER

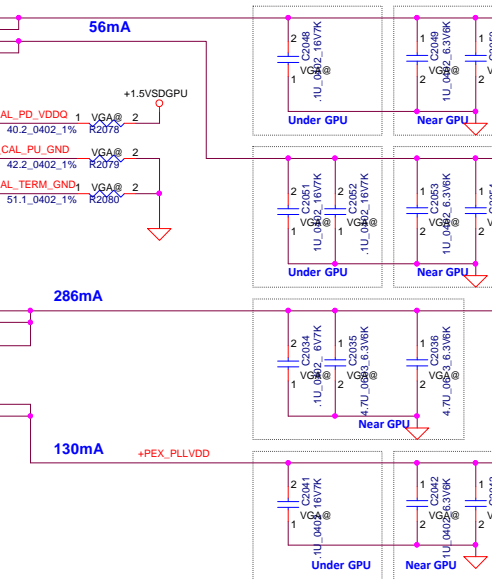
V7
W7
AA6
W6
Y6
M7
N7
T6
F6
T7
R7
U6
R6
J7
K7
K6
H6
J6

M7
N7
T6
F6
T7
R7
U6
R6
J7
K7
K6
H6
J6

T7
R7
U6
R6
J7
K7
K6
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J6

J7
K7
K6
H6
J6

GM108-ES-S-A1_FCBGA595



NV 16x DG-07158-V05

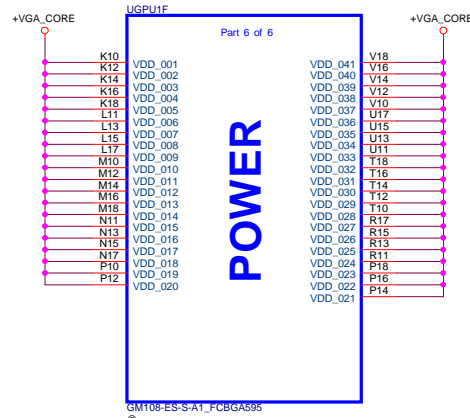
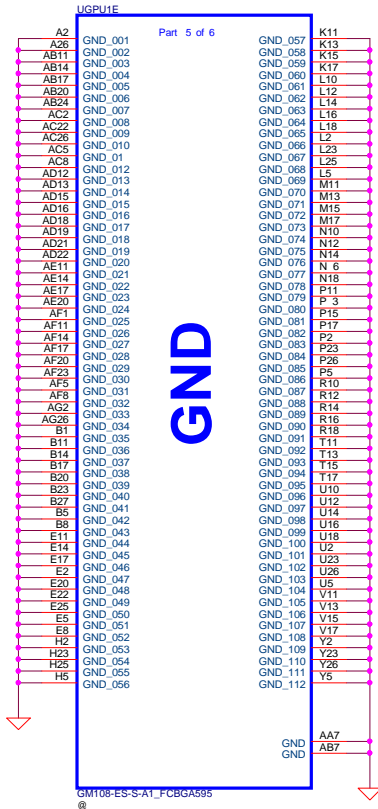
Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μ F	X7R	0402	1	Near GPU
4.7 μ F	X5R	0603	2	Near GPU

NV 16x DG-07158-V05

Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU



NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64 / GB2-64	4.7 μ F X6S	0603	10	10	Under GPU
	1 μ F X6S	0402	4	4	Under GPU
	47 μ F X5R	0805	1	1	Near GPU
	22 μ F X5R	0805	1	1	Near GPU
	4.7 μ F X5R	0805	5	5	Near GPU
	330 μ F POS	7343	1	1	Near GPU ESR \leq 6 m Ω

DA-07751-V01

Table 6. EDP-Peak³

Products	VRAM Type	GPU Core	GPU FBIO		FB Total ^{1,5}		1.05V Total ²
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴
		(A)	(A)	(A)	(A)	(A)	(A)
N16V-GMR1	GDDR5	30.0	-	2.9	-	6.8	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

Notes:

1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
2. 1.05V Total includes the PCIe and other 1.05V power rails.
3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
4. Power supply rail voltages set to maximum DC tolerance.
5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

DA-07314-V04

Table 6. EDP-Peak³

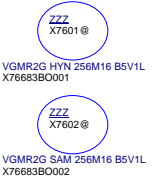
Products	VRAM Type	GPU Core	GPU FBIO		FB Total ^{1,5}		1.05V Total ²
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴
		(A)	(A)	(A)	(A)	(A)	(A)
N16V-GM	DDR3/L	40.97	3.87	3.34	5.86	4.96	1.74

Notes:

1. FB Total = GPU FBIO + VRAM IO + VRAM Core = FBVDD + FBVDDQ
2. 1.05V Total includes the PCIe and other 1.05V power rails.
3. Worst case current is observed at the temperature of the GPS Thermal Control Limit defined in Table 3.
4. Power supply rail voltages set to maximum DC tolerance.
5. VRAM Total power is for reference only. For absolute ratings, please contact VRAM manufacturer.

VRAM DDR3 chips

X76 for GMR1 2G



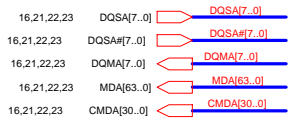
X76 for GMR1 4G



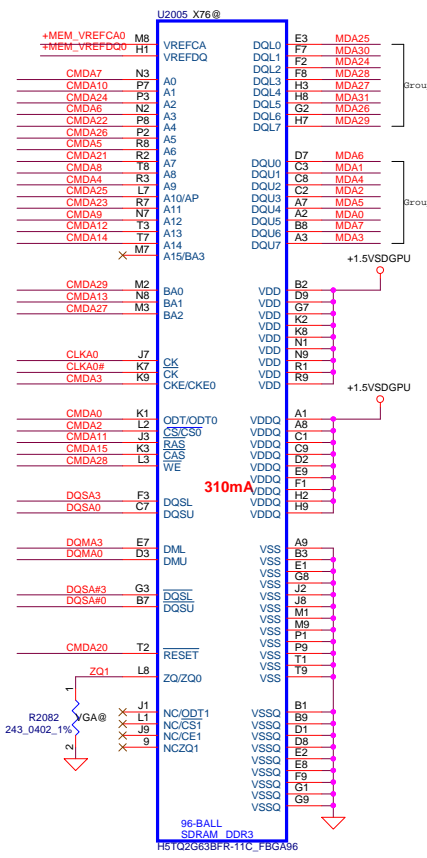
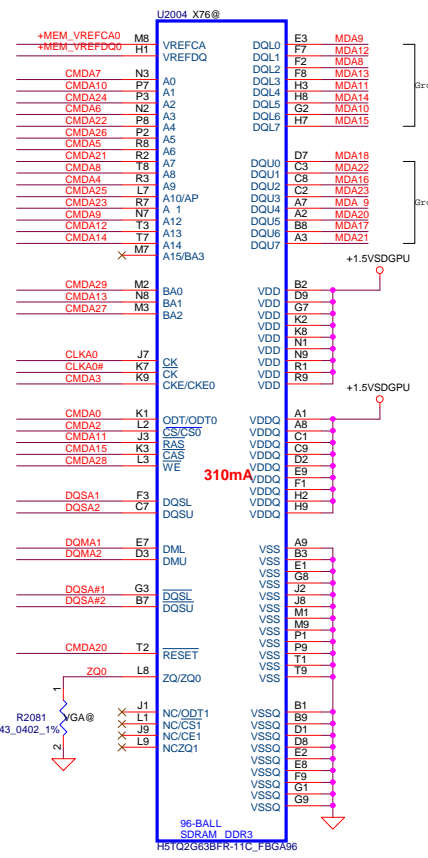
X76 for GTR 2G



X76 for GTR 4G



Lower Rank 0 BOT SIDE

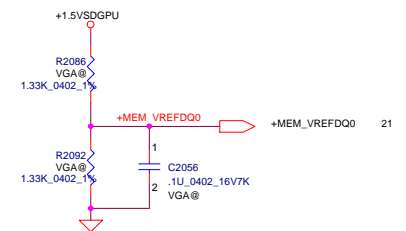
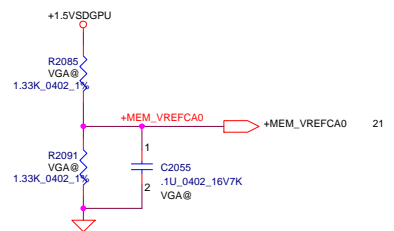
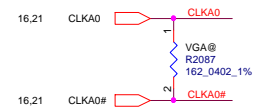
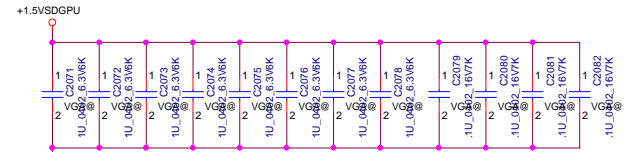


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17			CS1*	
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

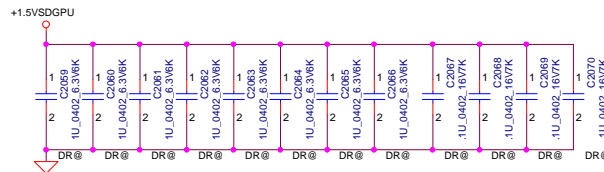
Capacitor Type		Population		Location
		FBVDDQ	FBVDD	
FBVDD/Q Combined				
0.1 µF	X7R	0402	2	Under DRAM
1.0 µF	X7R	0603	4	Under DRAM
10 µF	X5R	0805	0	Close to DRAM



16,20,22,23	DQSA[7..0]		DQSA[7..0]
16,20,22,23	DQSA# [7..0]		DQSA# [7..0]
16,20,22,23	DQMA[7..0]		DQMA[7..0]
16,20,22,23	MDA[63..0]		MDA[63..0]
16,20,22,23	CMDA[30..0]		CMDA[30..0]

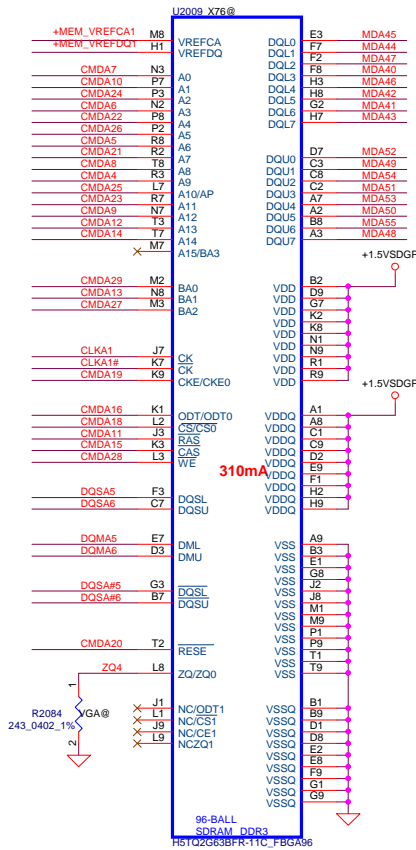
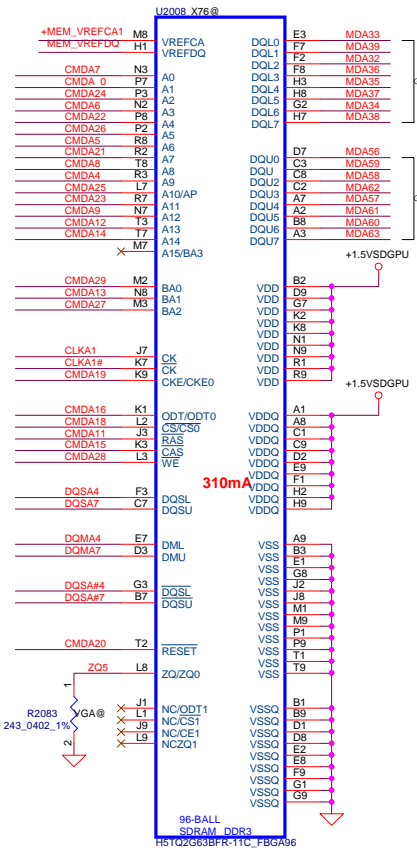
Pin configuration diagram for the H5TQ2G63BFR-11C FBGA96 package. The package is a 16x16 grid. The top row (A0 to A15) is connected to the VREFCA and VREFDQ pins. The bottom row (T0 to T9) is connected to the VSS and VSSQ pins. The left side (P0 to P9) is connected to the VDD and VDDQ pins. The right side (N0 to N9) is connected to the VDD and VDDQ pins. The center pins (M0 to M9) are connected to the VDD and VDDQ pins. The package is labeled 'H5TQ2G63BFR-11C FBGA96'.

	Command Bit	Default Pull down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



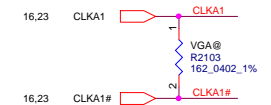
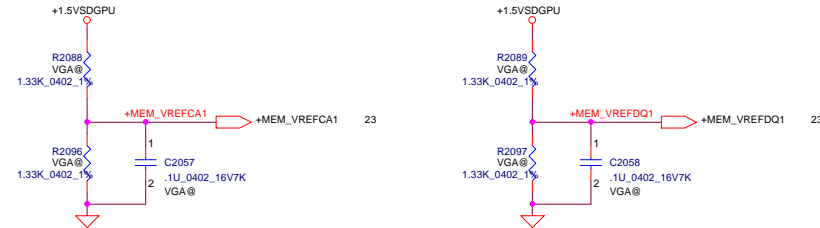
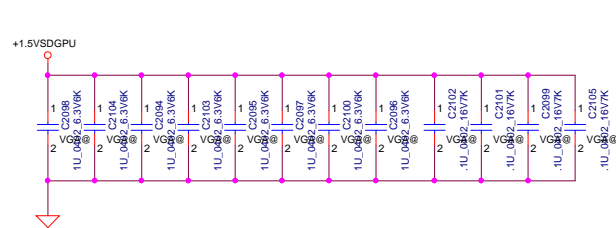
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/12/24	Deciphered Date	2017/12/24	Title		
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				Size	Document Number	Rev
				Cust	1.0	
				B5V1L Braswell-M/B LA-D921P		
				Date	Wednesday May 11 2016	Sheet 21 of 52

16,20,21,23	DQSA[7..0]		DQSA[7..0]
16,20,21,23	DQSA#[7..0]		DQSA#[7..0]
16,20,21,23	DQMA[7..0]		DQMA[7..0]
16,20,21,23	MDA[63..0]		MDA[63..0]
16,20,21,23	CMDA[30..0]		CMDA[30..0]



Mode & Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



16,20,21,22	DQSA[7..0]		DQSA[7..0]
16,20,21,22	DQSA#[7..0]		DQSA#[7..0]
16,20,21,22	DQMA[7..0]		DQMA[7..0]
16,20,21,22	MDA[63..0]		MDA[63..0]
16,20,21,22	CMDA[30..0]		CMDA[30..0]

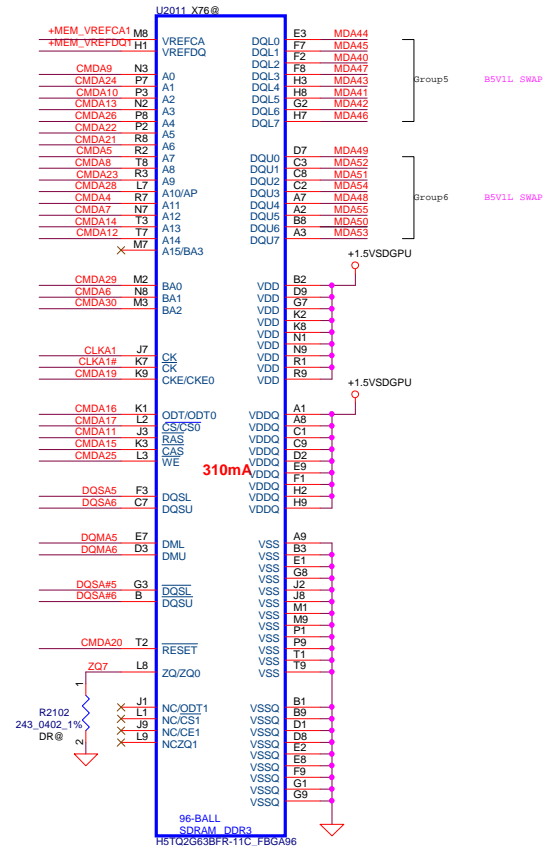
U2010_X76e

Group 4

Pin	Signal	Pin	Signal
1	VREFCA1	15	DQ0
2	VREFDQ1	16	DQ1
3	CMDA24	17	DQ2
4	CMDA28	18	DQ3
5	CMDA10	19	DQ4
6	CMDA13	20	DQ5
7	CMDA26	21	DQ6
8	CMDA22	22	DQ7
9	CMDA21	23	DQ8
10	CMDA5	24	DQ9
11	CMDA8	25	DQ10
12	CMDA23	26	DQ11
13	CMDA28	27	DQ12
14	CMDA4	28	DQ13

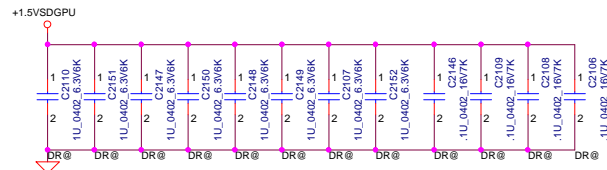
Group 7

Pin	Signal	Pin	Signal
15	CMDA17	31	DQ14
16	CMDA7	32	DQ15
17	CMDA14	33	DQ16
18	CMDA12	34	DQ17
19	M7	35	DQ18
20	CMDA29	36	DQ19
21	CMDA6	37	DQ20
22	CMDA30	38	DQ21
23	CLKA1	39	DQ22
24	CLKA1#	40	DQ23
25	CLKA19	41	DQ24
26	CMDA16	42	DQ25
27	CMDA17	43	DQ26
28	CMDA11	44	DQ27
29	CMDA15	45	DQ28
30	CMDA25	46	DQ29
31	DQSA4	47	DQ30
32	DQSA7	48	DQ31
33	DQMA4	49	DQ32
34	DQMA7	50	DQ33
35	DQSA4	51	DQ34
36	DQSA7	52	DQ35
37	CMDA20	53	DQ36
38	ZQ6	54	DQ37
39	R2090	55	DQ38
40	243.0402-1% DR	56	DQ39
41	J1	57	DQ40
42	J9	58	DQ41
43	L9	59	DQ42
44	NC/ODT1	60	DQ43
45	NC/CS1	61	DQ44
46	VSSQ1	62	DQ45
47	NC/Z1	63	DQ46
48	VSSQ	64	DQ47
49	VSSQ	65	DQ48
50	VSSQ	66	DQ49
51	VSSQ	67	DQ50
52	VSSQ	68	DQ51
53	VSSQ	69	DQ52
54	VSSQ	70	DQ53
55	VSSQ	71	DQ54
56	VSSQ	72	DQ55
57	VSSQ	73	DQ56
58	VSSQ	74	DQ57
59	VSSQ	75	DQ58
60	VSSQ	76	DQ59
61	VSSQ	77	DQ60
62	VSSQ	78	DQ61
63	VSSQ	79	DQ62
64	VSSQ	80	DQ63
65	VSSQ	81	DQ64
66	VSSQ	82	DQ65
67	VSSQ	83	DQ66
68	VSSQ	84	DQ67
69	VSSQ	85	DQ68
70	VSSQ	86	DQ69
71	VSSQ	87	DQ70
72	VSSQ	88	DQ71
73	VSSQ	89	DQ72
74	VSSQ	90	DQ73
75	VSSQ	91	DQ74
76	VSSQ	92	DQ75
77	VSSQ	93	DQ76
78	VSSQ	94	DQ77
79	VSSQ	95	DQ78
80	VSSQ	96	DQ79
81	VSSQ	97	DQ80
82	VSSQ	98	DQ81
83	VSSQ	99	DQ82
84	VSSQ	100	DQ83
85	VSSQ	101	DQ84
86	VSSQ	102	DQ85
87	VSSQ	103	DQ86
88	VSSQ	104	DQ87
89	VSSQ	105	DQ88
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94</			

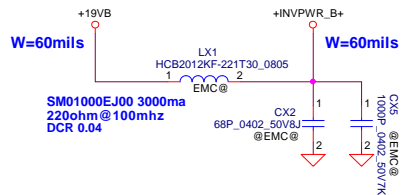
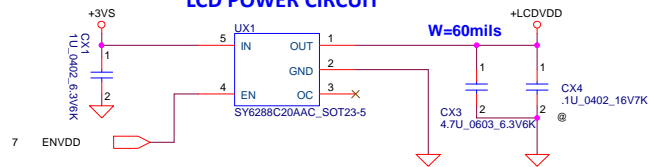


Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

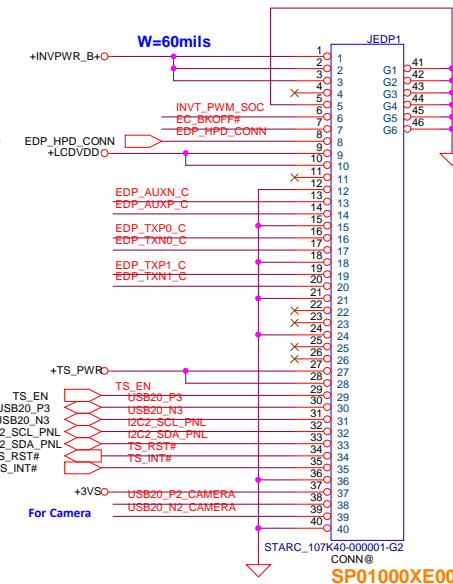
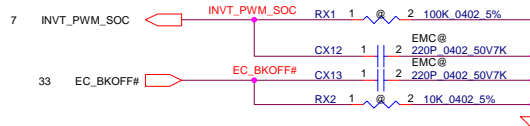
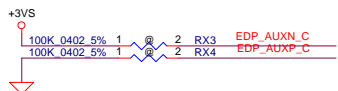
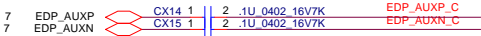
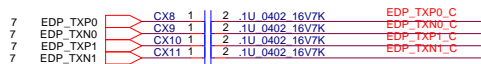
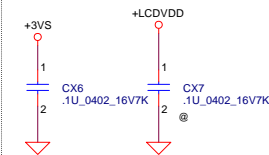
	Command Bit	Default Pull down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



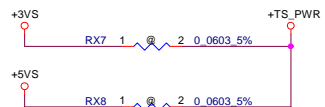
LCD POWER CIRCUIT



Place closed to JEDP1



Touch Screen



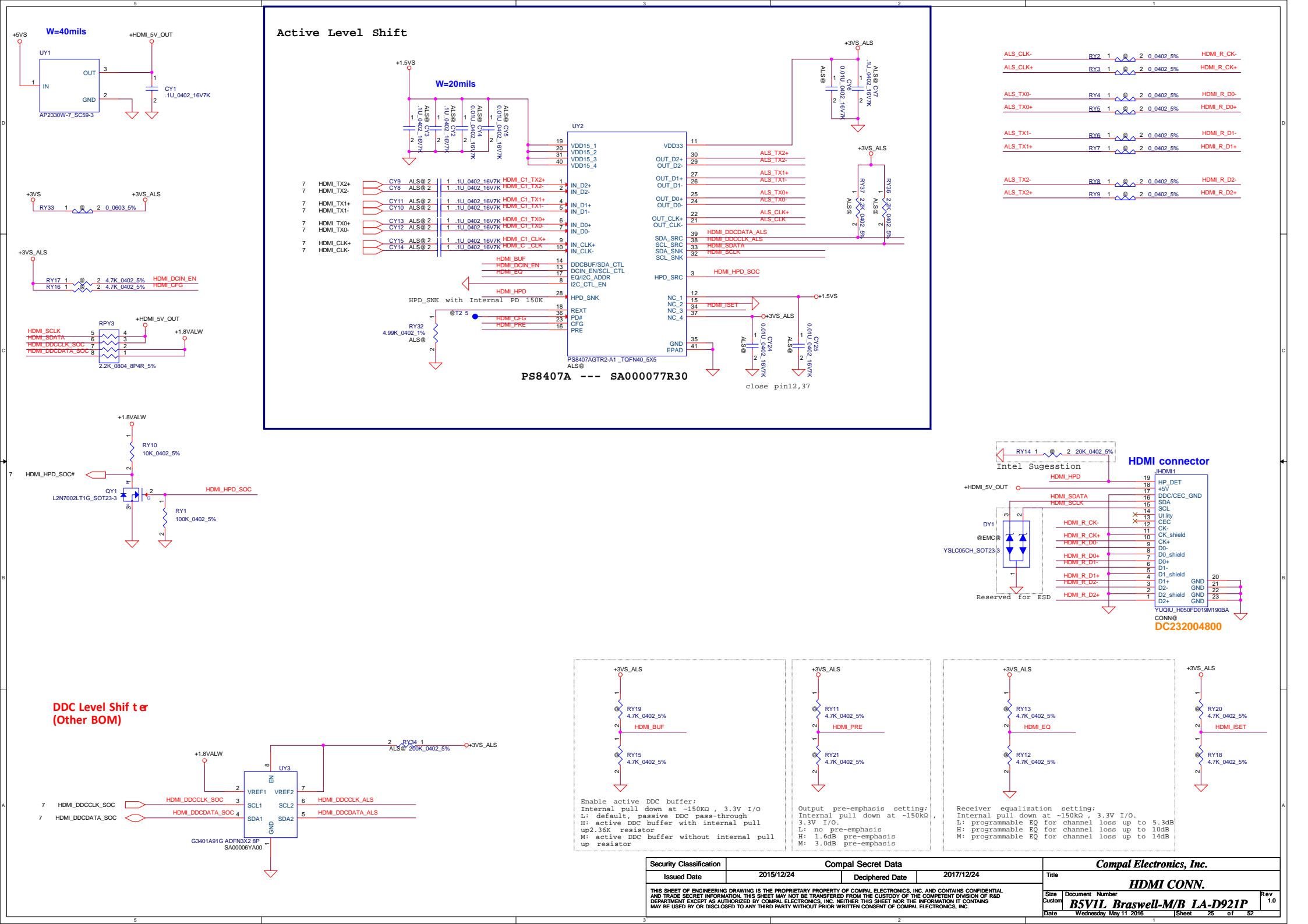
Camera



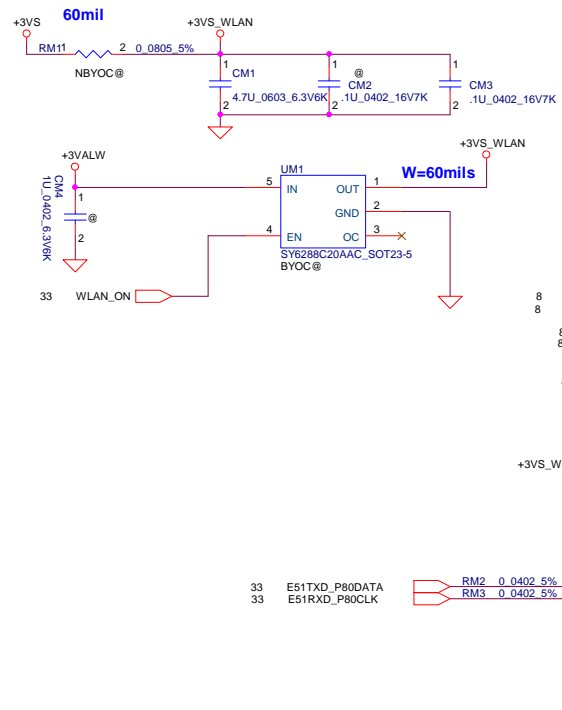
follow B5W1A they confirmed with EMC team no need to reserve choke

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2015/12/24				Title			
				Deciphered Date				eDP CONN.			
				2017/12/24				Size			
								Custom			
								B5V1L Braswell-M/B LA-D921P			
								Date			
								Wednesday May 11 2016			
								Sheet			
								24 of 52			
								Rev			
								1.0			

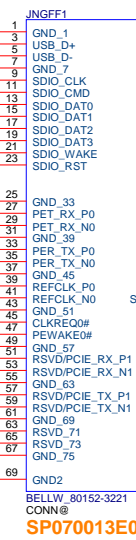
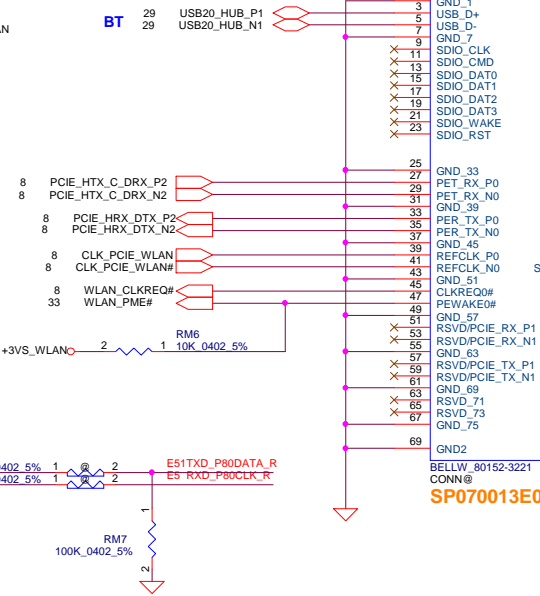
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For Wireless LAN



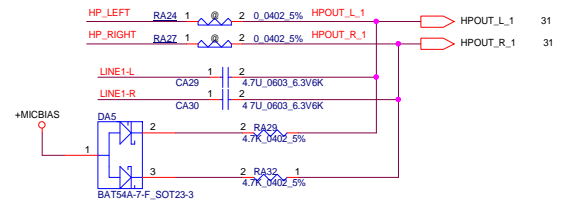
BT



NGFF WL+BT (KEY E)

74	1.8V	GND	75
72	1.8V	RESERVED/REFCLK1	73
70	1.8V	RESERVED/REFCLK1	71
68	UM_Power_SRC/GPIO/PEWake1#	GND	69
66	UM_Power_SINK/CLKREQ#	Reserved/PEWk1	67
64	UM_SWP/PERST1#	Reserved/PEWk2	65
62	RESERVED	GND	63
60	ALERT# (IO/0.3V)	Reserved/PETx1	61
58	DC CLK (IO/0.3V)	Reserved/PETx1	59
56	DC DATA (IO/0.3V)	GND	57
54	W_DISABLE# (IO/0.3V)	PEWake# (IO/0.3V)	55
52	Reserved/W_DISABLE# (IO/0.3V)	CLKREQ# (IO/0.3V)	53
50	PERST0# (IO/0.3V)	GND	51
48	SUSCLK32KHz (IO/0.3V)	REFCLK0	49
46	CODEX1 (IO/0.1.8V)	REFCLK0	47
44	CODEX3 (IO/0.1.8V)	GND	45
42	VENDOR DEFINED	PEWk0	43
40	VENDOR DEFINED	PEWk0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (IO/0.1.8V)	PEWk0	37
34	UART CTS (IO/0.1.8V)	PEWk0	35
32	UART TX (IO/0.1.8V)	GND	33
30	UART RX (IO/0.1.8V)	SDIO Power# (IO/0.1.8V)	29
28	UART Wake# (IO/0.3V)	SDIO Wake# (IO/0.3V)	27
26	GND	SDIO DATA# (IO/0.1.8V)	25
24	LEDx2 (I/OOD)	SDIO DATA3 (IO/0.1.8V)	23
22	PCM_IN/IO/SD_IO (IO/0.1.8V)	SDIO DATA2 (IO/0.1.8V)	21
20	PCM_IN/IO/SD_IO (IO/0.1.8V)	SDIO DATA1 (IO/0.1.8V)	19
18	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	SDIO DATA0 (IO/0.1.8V)	17
16	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	SDIO CMD# (IO/0.1.8V)	15
14	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	SDIO CLK (IO/0.1.8V)	13
12	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	GND	11
10	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	GND	9
8	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	GND	7
6	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	GND	5
4	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	GND	3
2	PCM_SYNC/IO/SD_IO (IO/0.1.8V)	GND	1

SM01000EJ00 3000mA 220ohm@100mhz DCR 0.04



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Diagram 1: +3V_SOC connected to R270 (0.0402_5%) and C284 (10U_0003_6.3V6M). HUB@ is connected to the junction of R270 and C284.

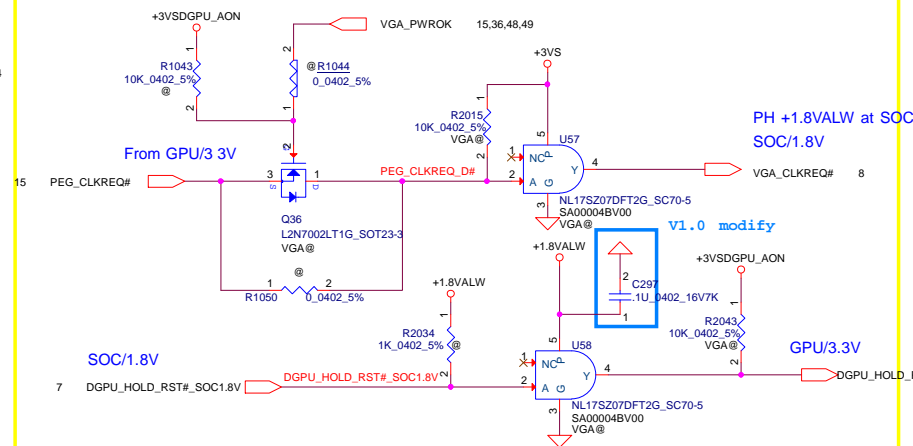
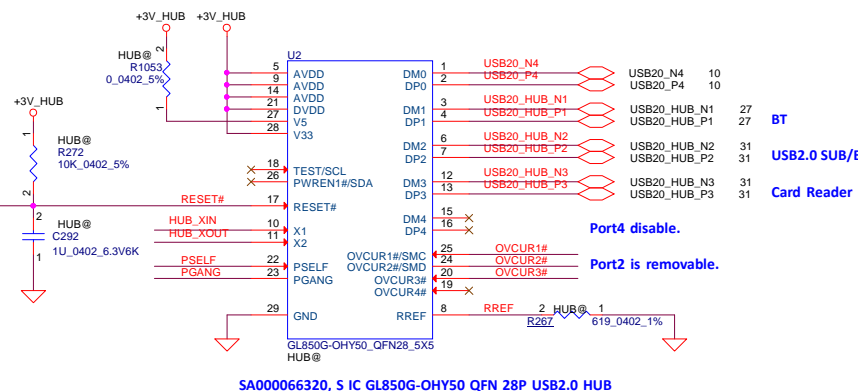
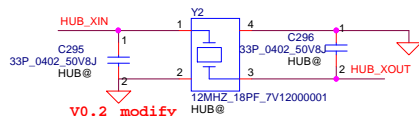
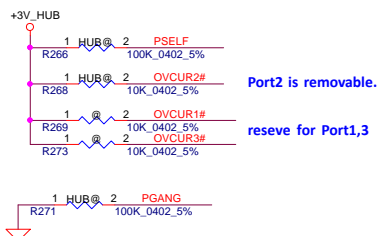
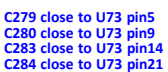
Diagram 2: +3V_HUB connected to C285, C289, C291, and C290 (all 0.1U_0402_16V7K). HUB@ is connected to the junction of C285 and C289.

Diagram 3: +3V_HUB connected to R266 (100K_0402_5%), R268 (10K_0402_5%), R269 (10K_0402_5%), and R273 (10K_0402_5%). HUB@ is connected to the junction of R266 and R268.

Diagram 4: +3V_HUB connected to R271 (100K_0402_5%). HUB@ is connected to the junction of R271 and the ground.

Annotations:

- Port2 is removable.
- reseve for Port1,3
- C279 close to U73 pin5
- C280 close to U73 pin9
- C283 close to U73 pin14
- C284 close to U73 pin21
- 33.41 SYSON
- V0.2 modify

[illegible]

TS LS (Other for BOM)

1.8V_ALW

10K_0402_5% R634

TS1@

TS_INT_R#

4

Y

NC U2511

TS_INT#

24

TS1@

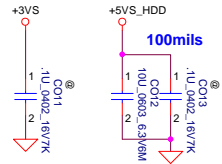
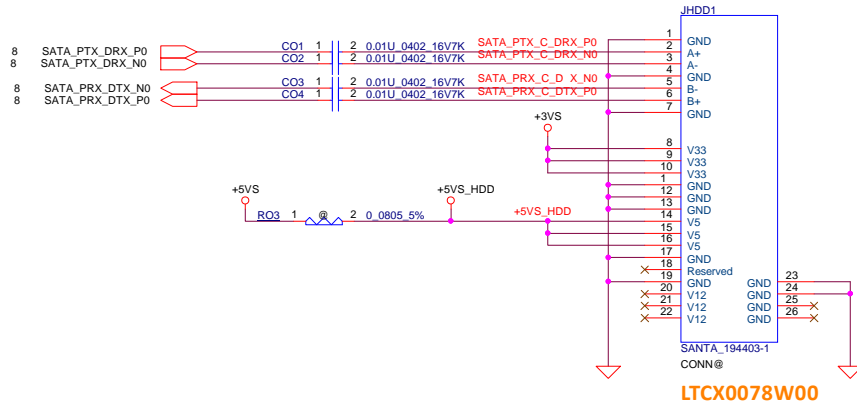
10K_0402_5% R635

+TS_PWR

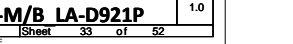
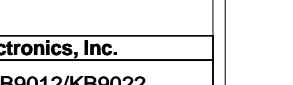
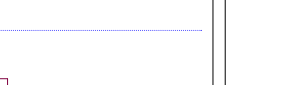
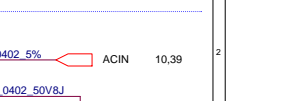
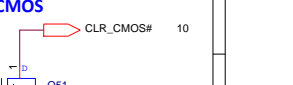
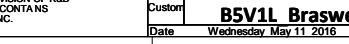
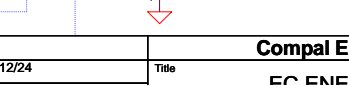
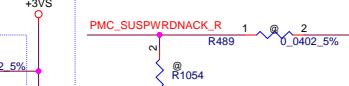
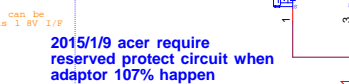
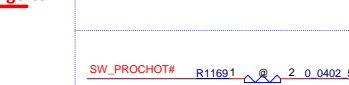
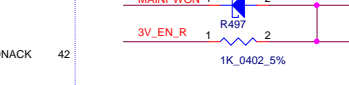
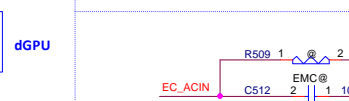
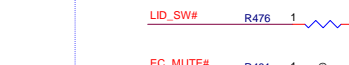
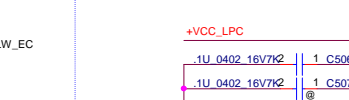
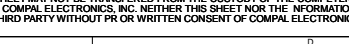
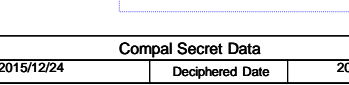
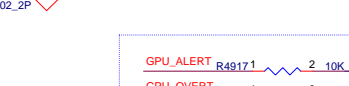
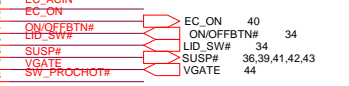
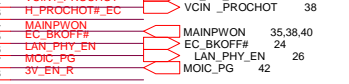
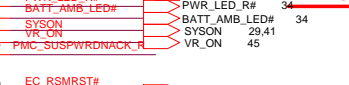
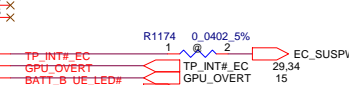
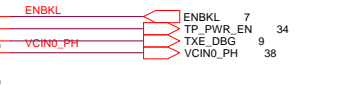
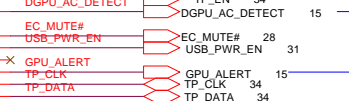
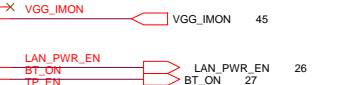
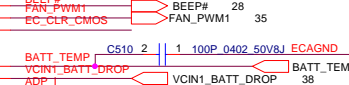
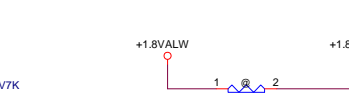
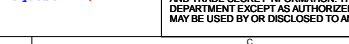
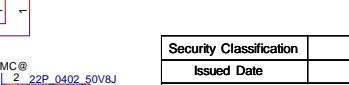
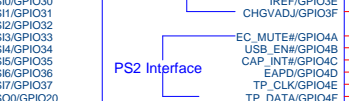
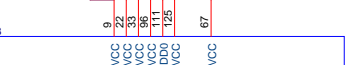
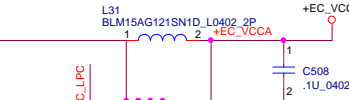
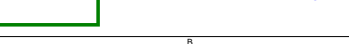
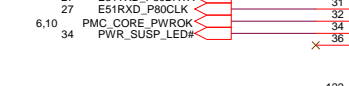
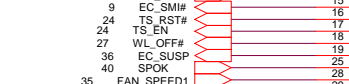
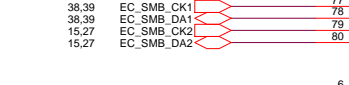
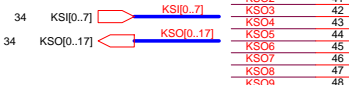
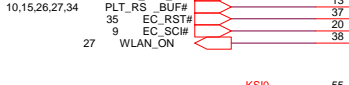
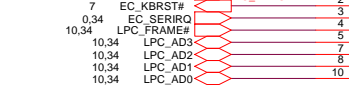
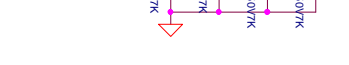
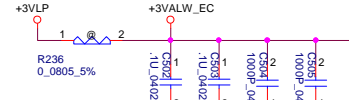
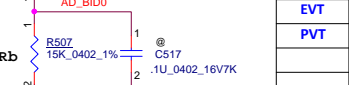
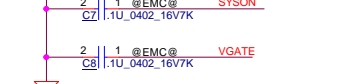
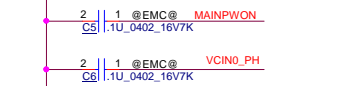
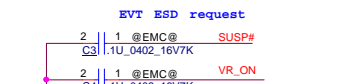
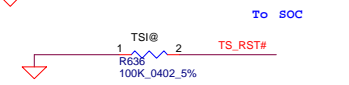
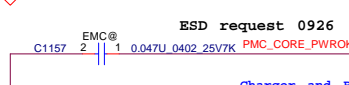
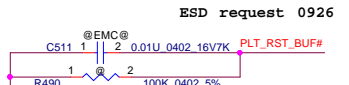
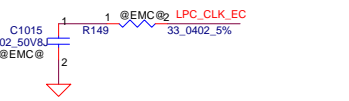
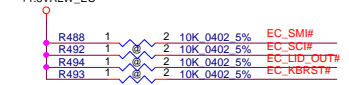
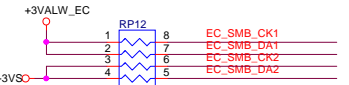
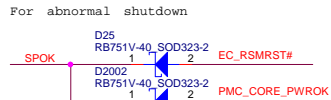
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SATA HDD1 Conn.



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								Date			Wednesday, May 11 2016	
								Sheet			30 of 52	



Board ID
Analog Board ID definition,
Please see page 3.

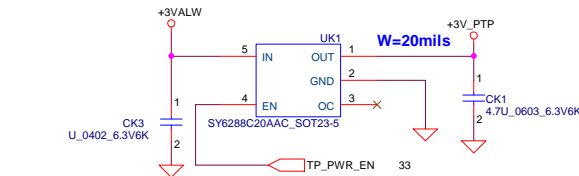
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For ESD request

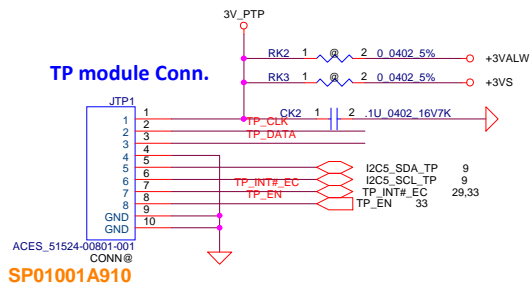
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EC ENE KB9012/KB9022			
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Date	Wednesday May 11 2016	Sheet	33 of 52

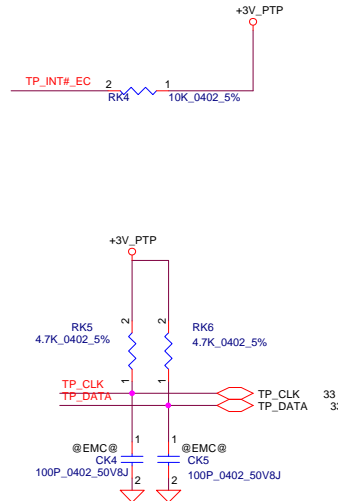
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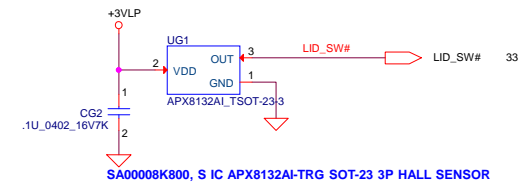
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SP01001A910

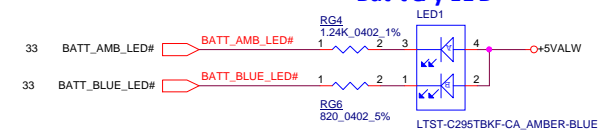


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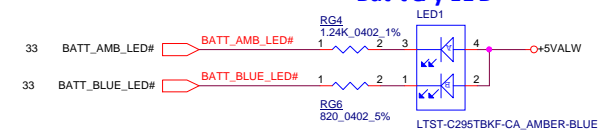


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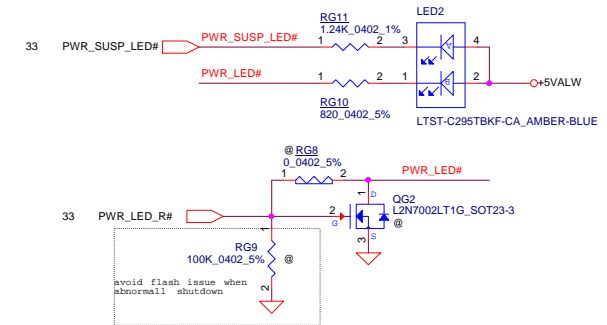
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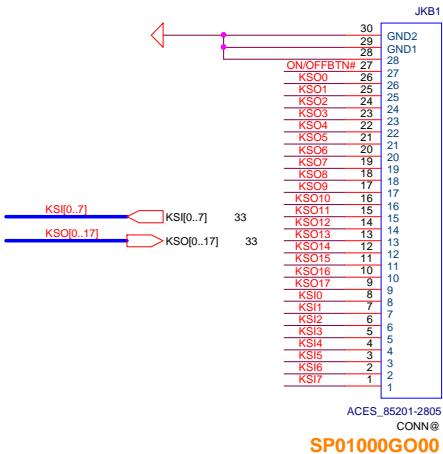
Bat tery LED



Power LED

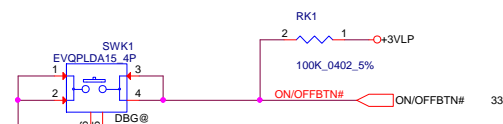


KB Conn.

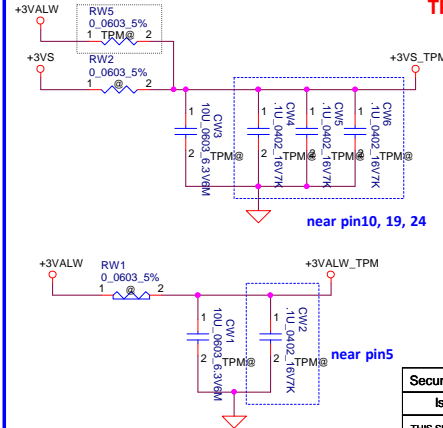


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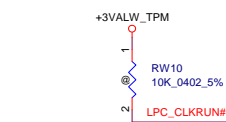
ON/OFF BTN Test only



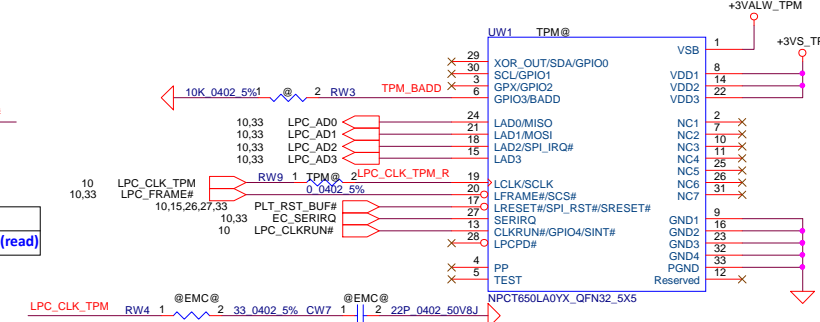
Follow B5W1A, prevent leakage



TPM Reserve



BADD	SELECTION
* 1	Ah(write), Afh(read)

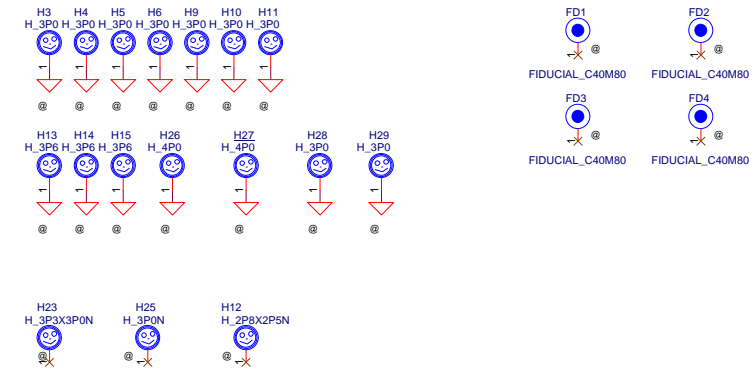


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2015/12/24				Title			
Deciphered Date				2017/12/24				KB/TP/LED/TPM/Screw Hole			
LPC_CLK_TPM				LPC_FRAME#				B5V1L Braswell-M/B LA-D921P			
LPC_CLK_TPM				LPC_CLK_TPM				Rev 1.0			
LPC_CLK_TPM				LPC_CLK_TPM				Date Wednesday May 11 2016			
LPC_CLK_TPM				LPC_CLK_TPM				Sheet 34 of 52			

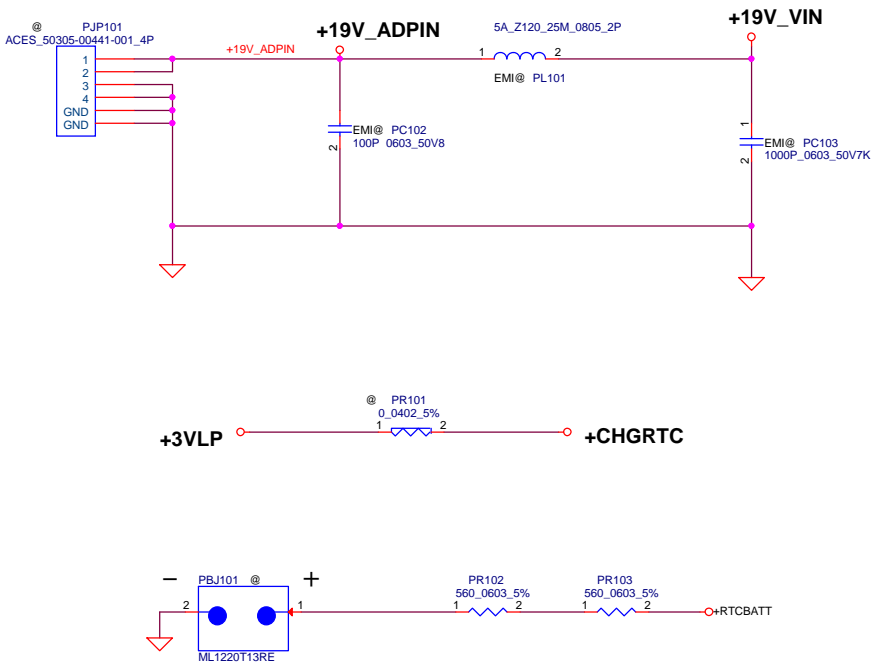
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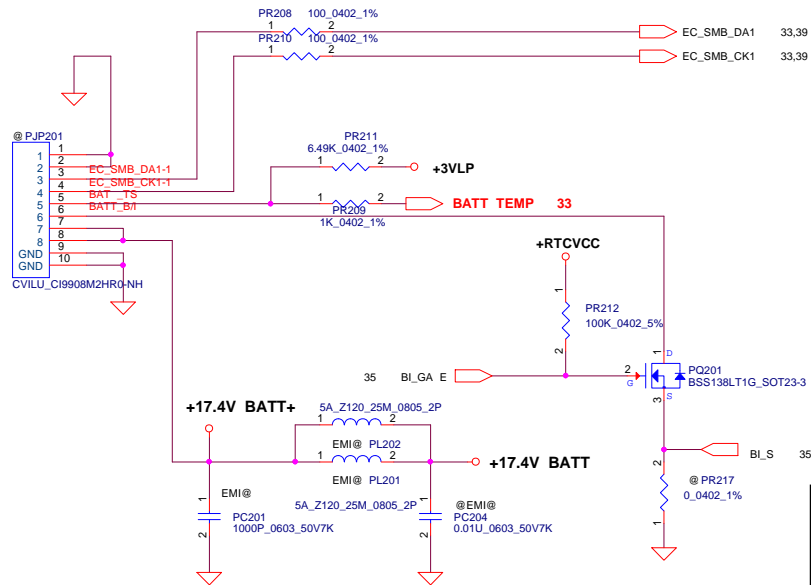
Screw Hole

[illegible]

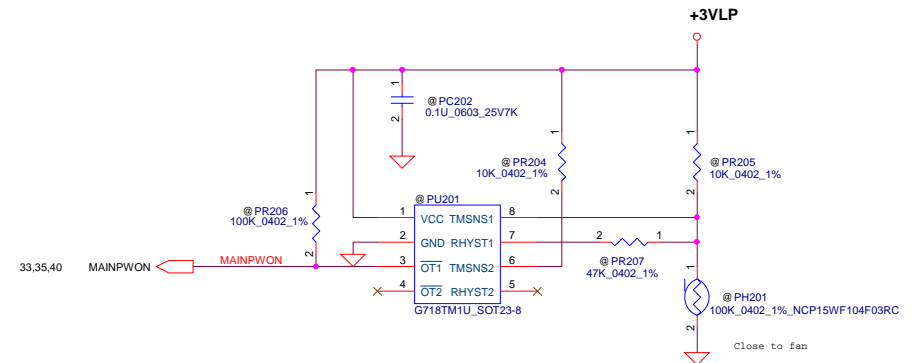
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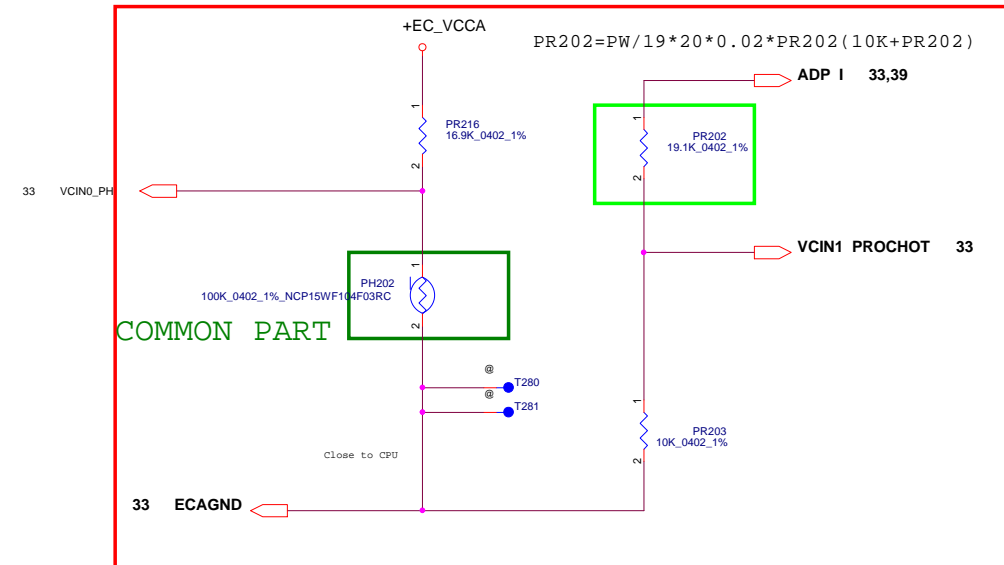
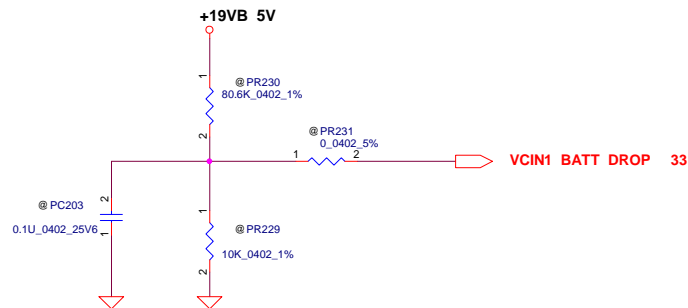


	For KB9022 OTP
9 2 °C	1.0V
5 6 °C	2.0V
PR216	16.9K ohm



Need confirm the setting

For KB9022 sense 20mΩ	Active	Recovery	PR202
65W	0.61V(58.5W)	0.47V(45W)	19.1KΩ
45W	0.61V(58.5W)	0.47V(45W)	10KΩ



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Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$VILIM = 20 * ILIM * Rsr$
 $ILIM = 3.3 * 100 / (100 + 316) / 20 / 0.01 = 3.966 A$

$ILIM * 0.01 * 20 (IC \text{ Current sense amplifier gain}) = VPR311 * 20 = +3VALW * 100 (PR317) / (100 + 316)$

Security Classification

Security Classification	Compal Secret Data
Issued Date	2015/12/24
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Compal Electronics, Inc.

Charger

B5V1L Braswell-M/B LA-D921P

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V
VILIM =	20*ILIM*Rsr		
ILIM =	3.3*100/(100+316)/20/0.01		
	= 3.966 A		

$$\text{ILIM} \times 0.01 \times 20 (\text{IC Current sense amplifier gain}) = \text{VPR311} \times 20 = +3\text{VALW} \times 100 (\text{PR317}) / (100 + 316)$$

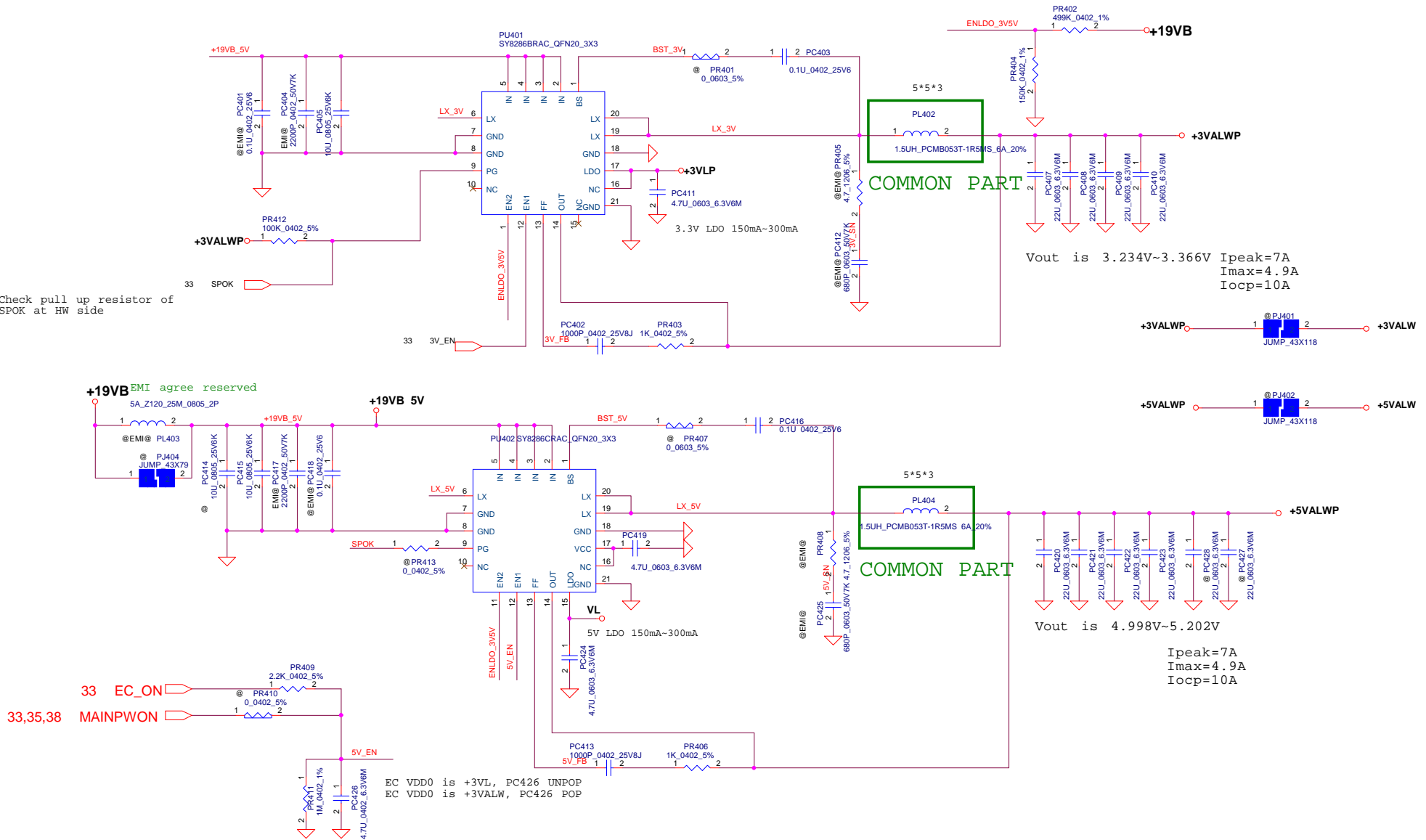
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						Size	Document	Number	Rev 1.0	
						Custom	B5V1L Braswell-M/B LA-D921P			
						Date	Wednesday, May 11, 2016		Sheet	39

Module model information

SY8208B_V2.mdd

SY8208C_V2.mdd

Check pull up resistor of
SPOK at HW side

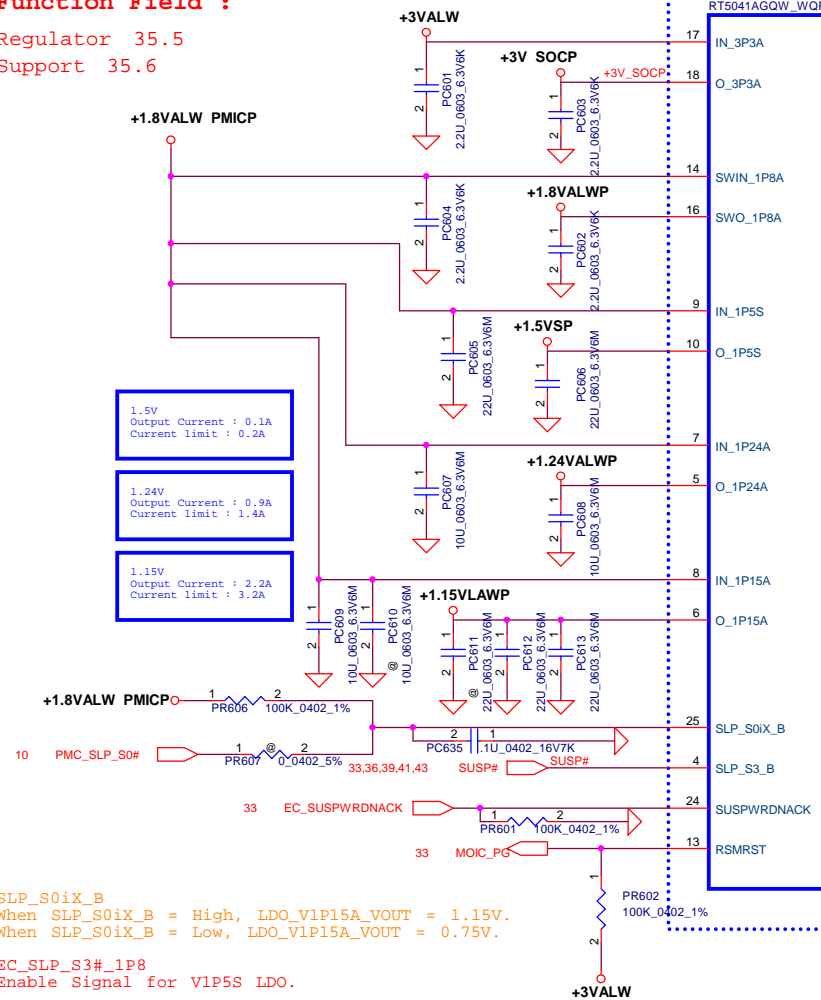


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Function Field :

Regulator 35.5

Support 35.6



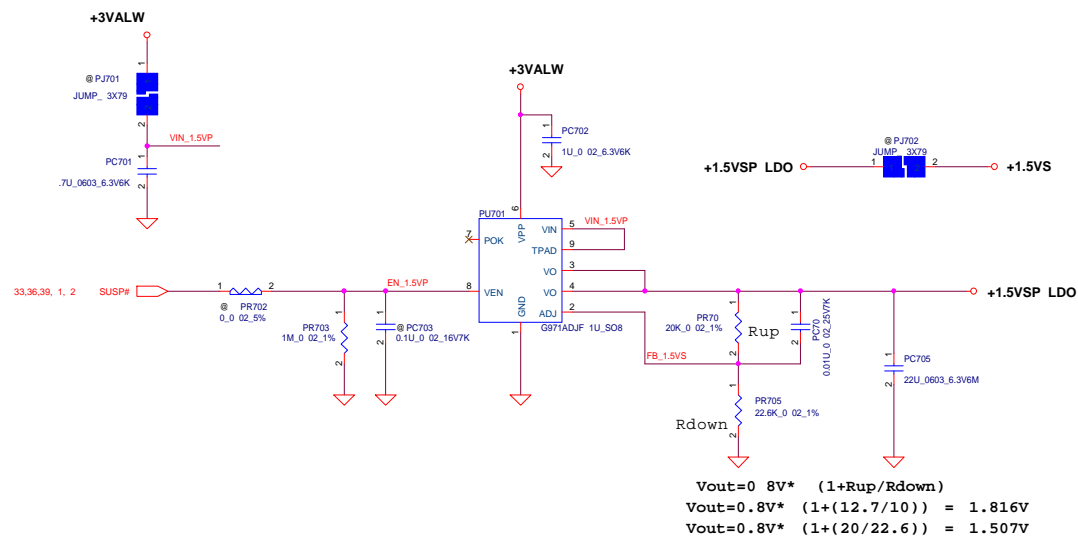
SLP_S0iX_B
When SLP_S0iX_B = High, LDO_V1P15A_VOUT = 1.15V.
When SLP_S0iX_B = Low, LDO_V1P15A_VOUT = 0.75V.

EC_SLP_S3#_1P8
Enable Signal for V1P5S LDO.

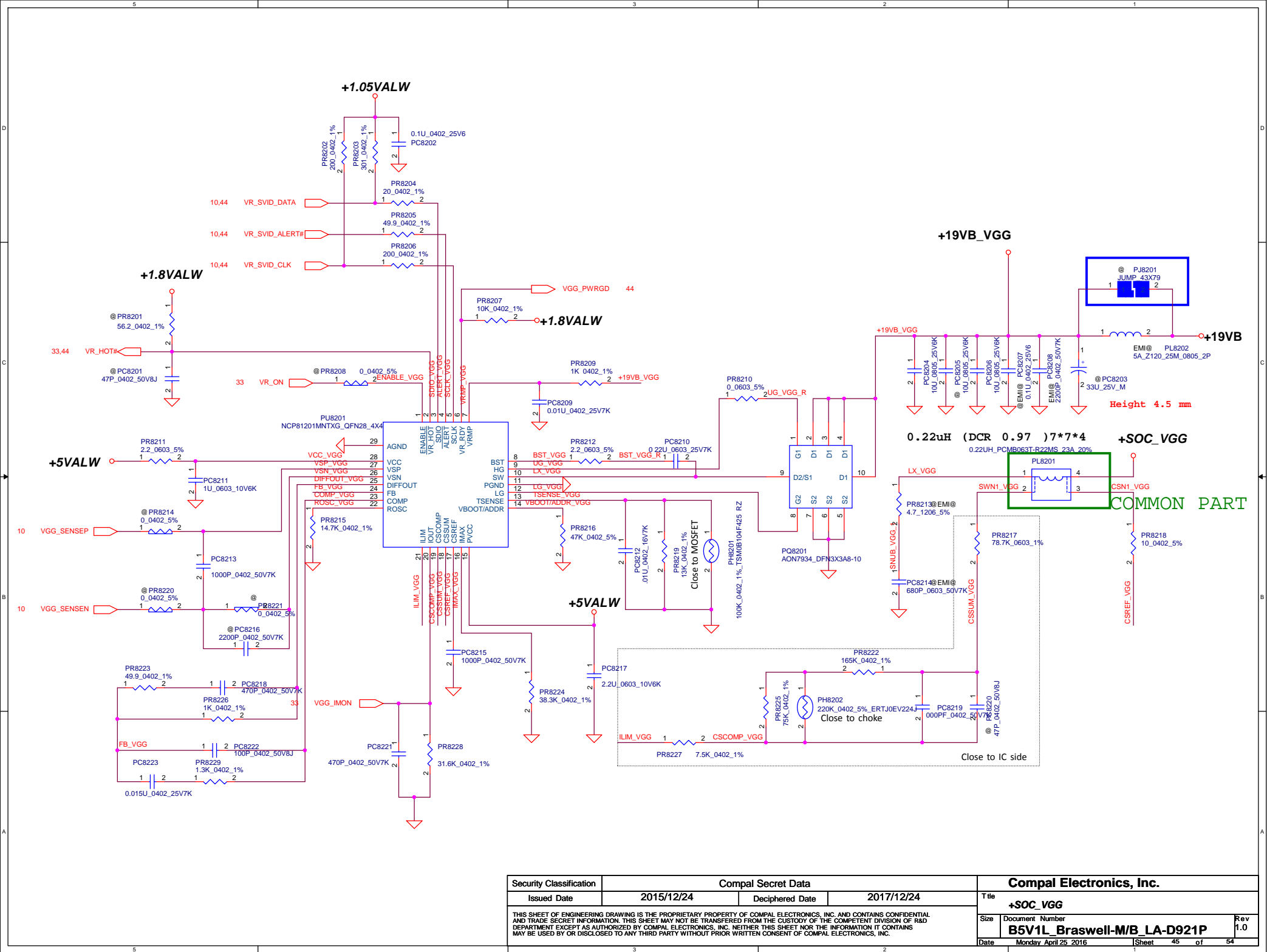
SUSPWRDNACK
HIGH:Disable Signal for All Power Rails.

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schematic from A4WAS
IC change to G971

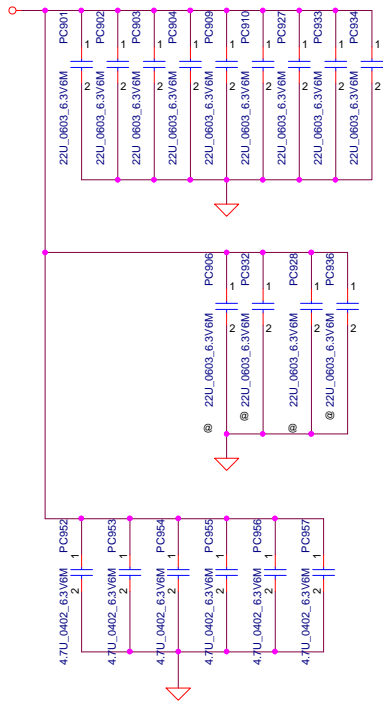


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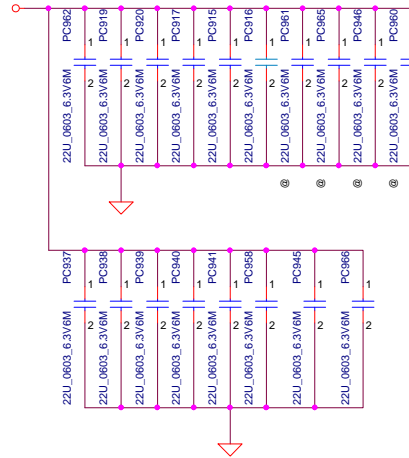
4.7U_0402 * 6 +22U_0603 * 15 + 4 reserved

+SOC_VCC



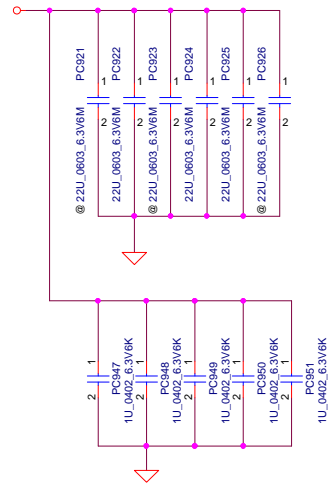
22U_0603 * 24 + 4 reserved

+SOC_VGG



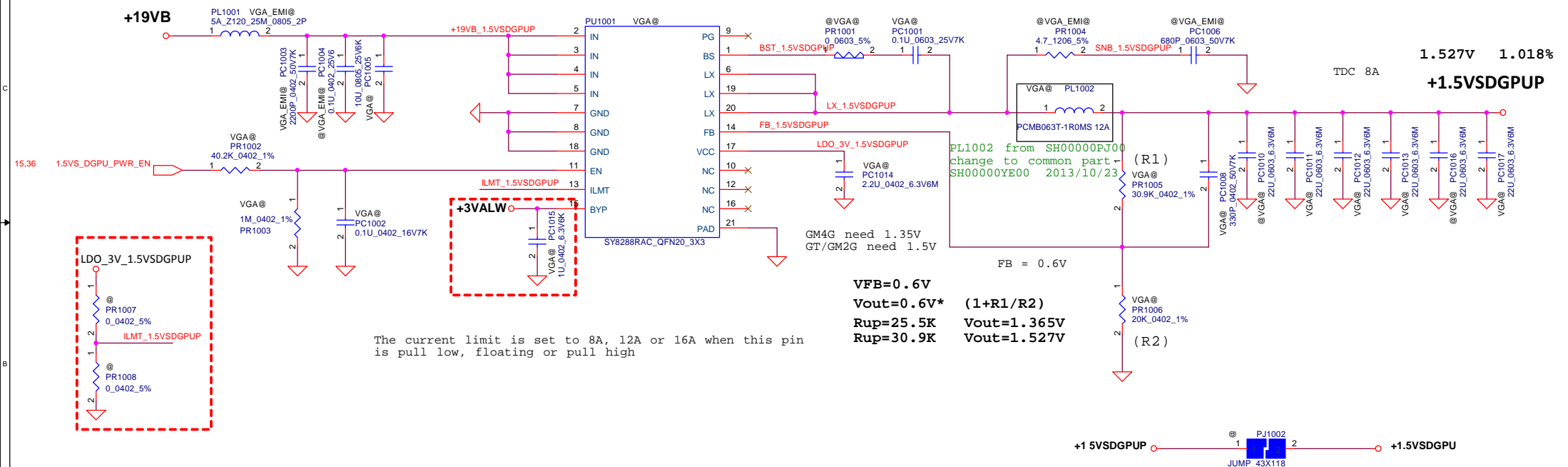
1U_0402 * 5+ 22U_0603*6 reserved

+1.05VALW



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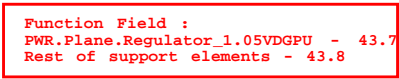
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



Module model information
SY8208D_V1.mdd

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```
Module model information
SY8032_V2.mdd
```


$$\begin{aligned} V_{out} &= 0.6V * (1 + R_{up}/R_{down}) \\ &= 0.6V * (1 + (7.68/10)) = 1.061 \quad (1.01\%) \\ &= 0.6V * (1 + (7.87/10)) = 1.072 \quad (2.1\%) \end{aligned}$$

Module model information
RT8813A V1A for IC module
RT8813A V1B for SW module

PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

$V_{boot} = V_{ref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$
 $V_{min} = V_{ref} * R_{ref2} / (R_{ref2} + R_{boot}) * [R_u / (R_{ref1} + R_t)]$
 $V_{max} = V_{ref} * R_{ref2} / (R_{ref1} / R_{refadj} + R_{boot} + R_{ref2})$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM-VID Spec and component Values

PWM-VID Spec	Config B	Config C	Config D
V _{min}	0.6V	0.65V	0.9V
V _{max}	1.2V	1.15V	1.15V
V _{boot}	0.9V	0.9V	1.028V
Voltage	6.25mV	25mV	12.5mV
N of Voltage	96	20	20
R _{refadj}	PR1209	20K	39K
R _{ref1}	PR1208	20K	30K
R _{boot}	PR1211	2K	3K
R _{ref2} =PR1210	PR1210	18K	24K
PR1224	PR1224	0	3K
C	PC1210	2.7nF	1.8nF

N16S-GT
N16S-GT
N16V-GM
N16V-GMR1
N16S-GTR

Current Limit setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10uA$

$I_{ripple} = (19.0.9) * 0.9 / (304.89KHz * 0.36u * 19) = 7.811A$

OCP=54A/2=27A per phase
 $I_{valley} = 27A - 7.811A/2 = 23.1A$

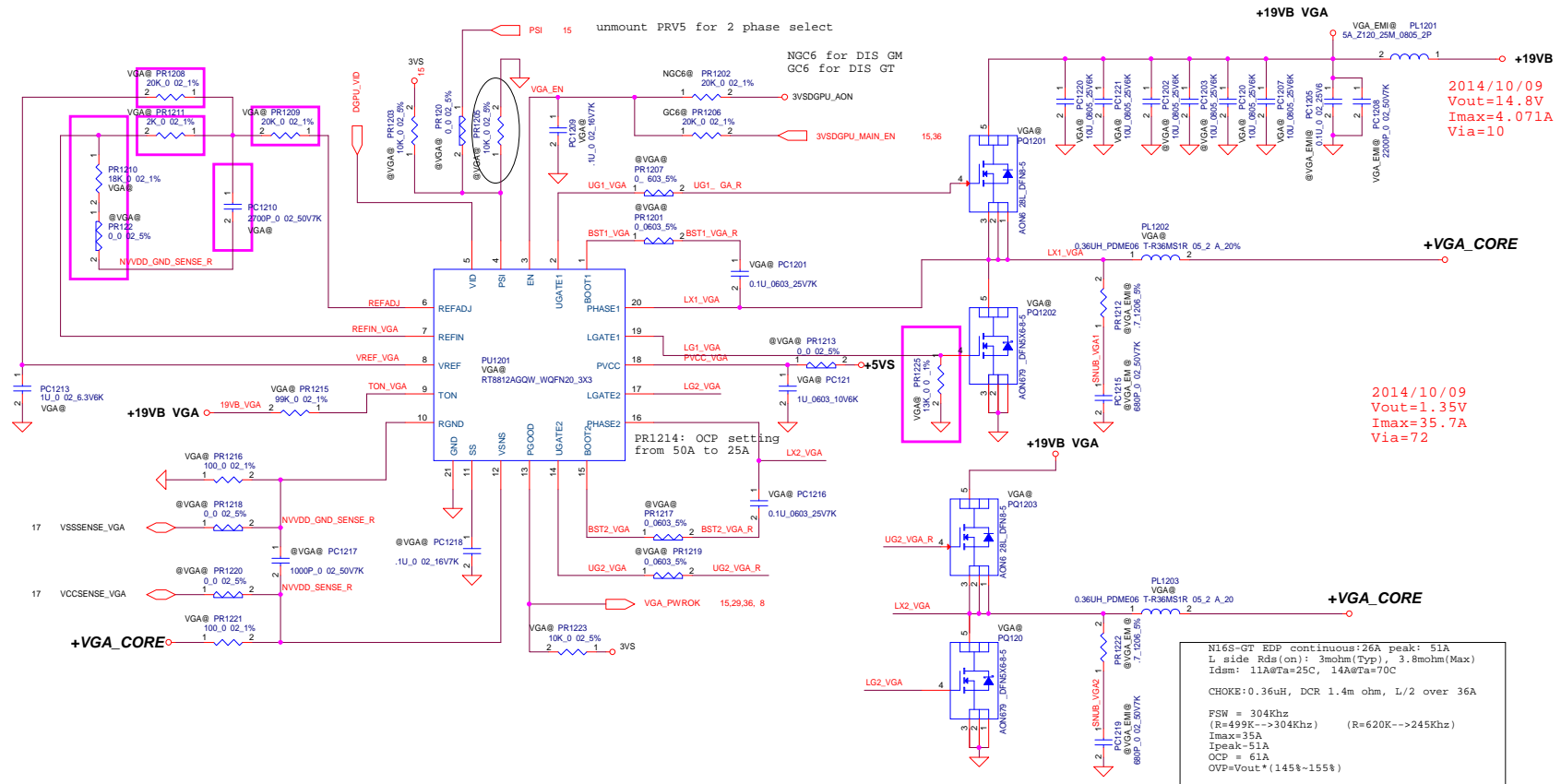
H-side MOS:AON6552
R_{ds(on)}:
5.6mohm @ V_{gs}=10V
6.7mohm @ V_{gs}=4.5V
Id :20A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
R_{dc}=0.97mohm +-5%
Heat Rating Current=34A
Saturation Current=25A

$C = 3 * 330uF (9mohm) = 990uF$
 $V_{ripple} = I_{ripple} * ESR(\text{min}) = 7.811A * 3mohm = 23.4mV$

Different VGA Chip (different EDP Max Current) need different solution

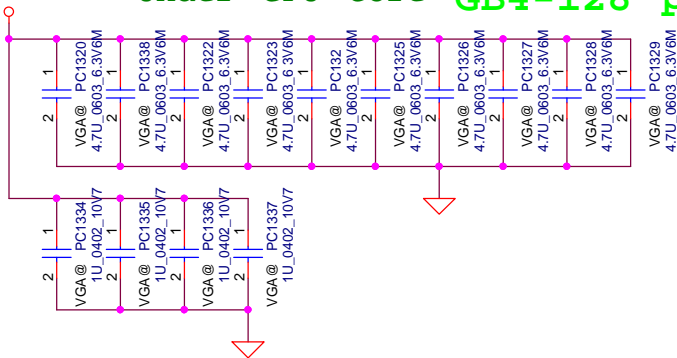
VGA	N16S-GTR	N16S-GT	N16V-GMR1	N16V-GM		N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B		Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	23W	23W	16W	24W		25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C						N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	26A	26A	18.5A	29.62A		27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	51A	51A	30A	40.97A		40A	60A	75A	60A	44.3A
Istep max (E situation)	38.5A	36.36A	20A	33.31A		12A	31.5A	35A		
OCP Setting Current						48A	72A	90A	72A	54A
Rocset						9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L		2phase 1H1L	2phase 1H2L 6mohm * 3 (L=0.22uH)	2phase 1H2L 4.5mohm * 3 (L=0.15uH)	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)						6mohm * 2				
Or OSCON (990uF)						10mohm * 2	NULL	NULL	GT@	GM@



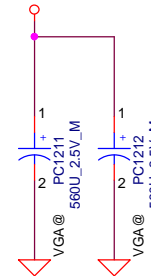
Remove GPU OTP circuit for HW request

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+VGA_CORE Under GPU Core GB4-128 package



+VGA_CORE

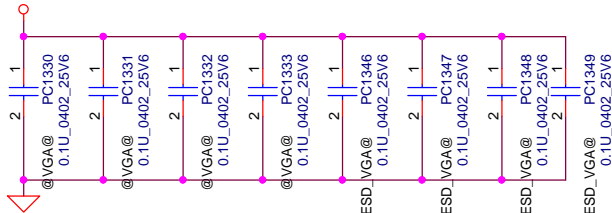


N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

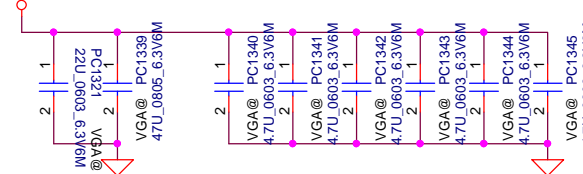
N15x 2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x 2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs(2PCS unpop)
4.7uF_0805_5pcs

+VGA_CORE



+VGA_CORE Near GPU Core



N15x 2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

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				Size	Document Number	Rev	
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				Size		Document Number		Rev
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